INTEGRATED DESIGN OF HIGH PERFORMANCE PULSED POWER CONVERTERS
APPLICATION TO KYSTRON MODULATORS FOR THE COMPACT LINEAR COLLIDER (CLIC)

Thèse

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Philosophiae Doctor (Ph. D.)

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Résumé

Ce travail de recherche présente l’étude, conception et validation d’une topologie de convertisseur de puissance pulsé qui compense la chute de tension pour des modulateurs de type klystron de haute performance. Cette topologie est capable de compenser la chute de tension du banc de condensateur principal et, en même temps, de faire fonctionner le modulateur avec une consommation de puissance constante par rapport au réseau électrique. Ces spécifications sont requises par le projet Compact Linear Collider (CLIC) pour les modulateurs klystron de son Drive Beam.

Le dimensionnement du système est effectué à partir d’un outil d’optimisation globale développé à partir des modèles analytiques qui décrivent les performances de chaque composant du système. Tous les modèles sont intégrés dans un processus optimal intermédiaire de conception qui utilise des techniques d’optimisation afin de réaliser un dimensionnement optimal du système. Les performances de cette solution optimale intermédiaire sont alors évaluées à l’aide d’un modèle plus fin basé sur des simulations numériques. Une technique d’optimisation utilisant l’approche «space mapping» est alors mise en œuvre. Si l’écart entre les performances prédites et les performances simulées est important, des facteurs de correction sont appliqués aux modèles analytiques et le processus d’optimisation est relancé. Cette méthode permet d’obtenir une solution optimale validée par le modèle fin en réduisant le nombre de simulations.

La topologie finale sélectionnée pour le cahier des charges du modulateur CLIC est validée expérimentalement sur des prototypes à échelle réduite. Les résultats valident la méthodologie de dimensionnement et respectent les spécifications.
Abstract

This research work presents the study, design and validation of a pulsed power converter topology that performs accurate voltage droop compensation for high performance klystron modulators. This topology is capable of compensating the voltage droop of the intermediate capacitor bank and, at the same time, it makes possible a constant power consumption operation of the modulator from the utility grid. These two main specifications are required for the Compact Linear Collider (CLIC) Drive Beam klystron modulators.

The dimensioning of the system is performed by developing a global optimization design tool. This tool is first based on developed analytical models describing the performances of each system subcomponent. All these models are integrated into an intermediate design environment that uses nonlinear optimization techniques to calculate an optimal dimensioning of the system. The intermediate optimal solution performances are then evaluated using a more accurate model based on numerical simulation. Therefore, an optimization technique using «space mapping» is implemented. If differences between predicted performances and simulated results are non-negligible, correction factors are applied to the analytical models and the optimization process is launched again. This method makes possible to achieve an optimal solution validated by numerical simulation while reducing the number of numerical simulation steps.

The selected final topology for the CLIC klystron modulator is experimentally validated using reduced scale prototypes. Results validate the selected methodology and fulfill the specifications.
Table of Contents

Résumé .................................................................................................................................. iii
Abstract .................................................................................................................................. iv
Table of Contents .................................................................................................................... v
List of Figures ........................................................................................................................ viii
List of tables ........................................................................................................................ xiv
List of symbols and abbreviations ....................................................................................... xv
Acknowledgments ................................................................................................................ 23
CHAPTER 1 ........................................................................................................................... 1
  1 INTRODUCTION .......................................................................................................... 1
    1.1 Framework ............................................................................................................... 2
    1.2 Project needs ............................................................................................................ 4
    1.3 PhD Objectives ......................................................................................................... 8
CHAPTER II ......................................................................................................................... 10
  2 STATE OF THE ART .................................................................................................. 10
    2.1 Klystron Modulators .............................................................................................. 10
    2.1.1 Polyphase converter modulator .......................................................................... 10
    2.1.2 ITER Gyrotron modulator ................................................................................ 11
    2.1.3 MARX modulator ............................................................................................. 13
    2.1.4 Jema modulator ................................................................................................. 14
    2.1.5 Modulator / Switching Buck Regulator ............................................................ 15
    2.1.6 Thomson modulator ......................................................................................... 16
    2.1.7 Monolithic transformer-based modulator .......................................................... 17
    2.1.8 Hard Switch modulator ..................................................................................... 19
    2.1.9 Matrix transformer modulator .......................................................................... 20
    2.1.10 SPRC Modulator ............................................................................................ 21
    2.2 Droop Compensators ............................................................................................ 22
    2.2.1 Passive Bouncer ................................................................................................. 23
    2.2.2 Active Bouncer .................................................................................................. 25
    2.2.3 Vernier Cells ....................................................................................................... 26
    2.2.4 Buck Regulator Cell ........................................................................................ 28
    2.2.5 Inductance capacitor type filter ......................................................................... 29
    2.3 Constant power consumption ................................................................................. 30
    2.4 High bandwidth – Low Ripple Power Converters ................................................. 32
      2.4.1 Multiphase buck converters ............................................................................. 33
      2.4.1.2 Topological solutions for high-bandwidth/low-ripple power converters ..... 34
      2.4.1.3 Design of high bandwidth output filter for multiphase buck converters .... 34
      2.4.1.4 Output filter inductances of multiphase buck converters ......................... 36
      2.4.1.5 Output Filter Topological Variants ............................................................. 37
      2.4.1.6 Output filter Linear Output Stage ............................................................... 38
      2.4.2 Control solutions for multiphase power converters ...................................... 39
CHAPTER V ........................................................................................................................ 89

4 DESIGN METHODOLOGY ........................................................................................ 40
4.1 Modulator and SPDC design challenge .............................................................. 41
4.1.1 Influence of the High Voltage Capacitor Charger Bandwidth ....... 41
4.1.2 Influence of main capacitor bank size ......................................................... 42
4.1.3 Influence of transformer droop ................................................................. 43
4.1.4 Conclusion on the design problem .............................................................. 43
4.2 Method Description.......................................................................................... 44

CHAPTER IV .................................................................................................................... 79
3 CONVERTER TOPOLOGY RESEARCH .................................................................. 79
3.1 Dual Purpose Active Bouncer DPAB ................................................................. 80
3.1.1 DPAB Ideal Operation .............................................................................. 80
3.1.2 DPAB Design ............................................................................................ 80
3.1.2.1 DPAB Output Filter ............................................................................. 80
3.1.2.2 Capacitor bank size .............................................................................. 81
3.1.3 DPAB Power Converter Topology .............................................................. 82
3.1.3.1 DPAB Control Strategy ......................................................................... 82
3.1.3.2 DPAB Simulation and performance evaluation ................................... 83
3.2 Split Power and Droop Compensator SPDC ................................................... 84
3.2.1 Fast Voltage Compensator FVC ................................................................. 84
3.2.2 FVC Design ............................................................................................... 85
3.2.2.1 FVC Output Filter Design ................................................................... 85
3.2.2.2 FVC Control strategy ........................................................................... 86
3.2.3 FVC Simulation and performance evaluation ........................................... 86
3.2.4 Active Bouncer ......................................................................................... 87
3.2.4.1 Active Bouncer Power Converter Topologies ....................................... 87
3.2.5 Active Bouncer Simulation and performance comparative analysis ........ 87
3.3 DPAB and SPDC comparative analysis ........................................................... 88
3.4 Selection and Conclusion ............................................................................... 89

CHAPTER III .................................................................................................................. 45
3 CONVERTER TOPOLOGY RESEARCH .................................................................. 45
3.1 Dual Purpose Active Bouncer DPAB ................................................................. 46
3.1.1 DPAB Ideal Operation .............................................................................. 46
3.1.2 DPAB Design ............................................................................................ 47
3.1.2.1 DPAB Output Filter ............................................................................. 47
3.1.2.2 Capacitor bank size .............................................................................. 48
3.1.3 DPAB Power Converter Topology .............................................................. 49
3.1.3.1 DPAB Control Strategy ......................................................................... 49
3.1.3.2 DPAB Simulation and performance evaluation ................................... 50
3.2 Split Power and Droop Compensator SPDC ................................................... 51
3.2.1 Fast Voltage Compensator FVC ................................................................. 51
3.2.2 FVC Design ............................................................................................... 52
3.2.2.1 FVC Output Filter Design ................................................................... 52
3.2.2.2 FVC Control strategy ........................................................................... 53
3.2.3 FVC Simulation and performance evaluation ........................................... 54
3.2.4 Active Bouncer ......................................................................................... 54
3.2.4.1 Active Bouncer Power Converter Topologies ....................................... 55
3.2.5 Active Bouncer Simulation and performance comparative analysis ........ 55
3.3 DPAB and SPDC comparative analysis ........................................................... 56
3.4 Selection and Conclusion ............................................................................... 57

CHAPTER V ........................................................................................................................ 89
5 DESIGN MODELS AND VALIDATION .................................................................... 89
5.1 Semiconductors Losses ................................................................................. 90
5.1.1 Power Switch Losses ................................................................................. 90
5.1.1.1 IGBT Conduction Losses ...................................................................... 91
5.1.1.2 IGBT Switching Losses ....................................................................... 91
5.1.2 Diode Losses ............................................................................................ 92
5.1.2.1 Diode Conduction Losses ................................................................... 92
5.1.2.2 Diode Reverse Recovery Losses ......................................................... 93
5.1.3 Linear operation losses ............................................................................. 94
5.2 Cooling ............................................................................................................ 95
5.2.1 Thermal equivalent model ....................................................................... 96
5.2.2 Steady-state thermal calculation method ................................................... 96

vi
5.2.3 Heat-sink calculation ................................................................. 114
5.3 Power switch lifetime .................................................................... 118
5.4 Inductance dimensioning model ..................................................... 122
5.5 Capacitor dimensioning model ....................................................... 124
5.6 Linear converter model for design purposes ................................. 126

CHAPTER VI ......................................................................................... 129
6 EXPERIMENTAL VALIDATION ....................................................... 129
6.1 Fast Voltage Compensator - FVC .................................................. 129
6.1.1 Modulator operation without FVC .............................................. 132
6.1.1.1 Capacitor charger operated in voltage control mode .......... 132
6.1.1.2 Capacitor charger operated in constant current control mode 134
6.1.2 Modulator operation with FVC .................................................... 136
6.2 Active Bouncer .............................................................................. 139
6.2.1 Experimental Validation ............................................................ 139
6.2.2 Comparison with numerical simulation results ......................... 157

CHAPTER VII ....................................................................................... 160
7 OPTIMAL DIMENSIONING OF THE FULL-SCALE CLIC KLYSTRON
MODULATOR ....................................................................................... 160
7.1 SPDC Active Bouncer ................................................................. 162
7.1.1 Optimization Phase 1: optimal voltage droop and switch technology 162
7.1.1.1 Optimization problem formulation ...................................... 162
7.1.1.2 Sensitivity analysis .............................................................. 167
7.1.1.3 Phase 1 Optimization results .............................................. 181
7.1.2 Optimization Phase 2: optimal voltage, number of phases, and IGBT model 185
7.1.3 Optimization Phase 3: correction and validation by numerical simulation 192
7.2 Fast Voltage Compensator FVC .................................................... 202
7.2.1 Optimization phase 1: number of phases and IGBT switch model 203
7.2.2 Optimization phase 2: correction and validation by numerical simulation 206

CONCLUSION AND FUTURE WORKS ................................................... 214
References .......................................................................................... 216

ANNEX A .............................................................................................. 224
A. Inductance dimensioning model .................................................... 224
   1 Inductance calculation ............................................................... 225
   2 Inductance losses estimation ..................................................... 227
   3 Inductance Thermal Modelling .................................................. 228
   4 Inductance volume ................................................................. 229
List of Figures

Figure 1 Layout of the Compact Linear Collider (CLIC) ................................................................. 2
Figure 2 Total output pulsed power delivered by CLIC klystron modulators synchronous operation ................................................................................................................................. 3
Figure 3 CLIC Drive-Beam Klystron Modulators International Collaboration ........................................ 4
Figure 4 Klystron Modulator block diagram ..................................................................................... 5
Figure 5 Performances definitions of the modulator output voltage pulse ........................................ 6
Figure 6 Polyphase converter modulator topology .............................................................................. 11
Figure 7 Elementary power module topology .................................................................................. 12
Figure 8 Gyrotron Modulator Topology ............................................................................................... 12
Figure 9 A) Marx Modulator topology. B) Charging circuit. C) Discharging circuit .......................... 13
Figure 10 Jema Modulator Topology .................................................................................................. 15
Figure 11 Modulator/Switching Buck Regulator Topology .............................................................. 16
Figure 12 Thomson Modulator topology ........................................................................................... 17
Figure 13 Modulator Topology based on a Monolithic Pulse Transformer ........................................ 18
Figure 14 CERN LINAC4 monolithic transformer modulator .......................................................... 19
Figure 15 Hard-Switch modulator topology ....................................................................................... 20
Figure 16 Matrix transformer modulator topology ............................................................................ 21
Figure 17 Individual SPRC module ..................................................................................................... 22
Figure 18 SPRC Modulator Topology .................................................................................................. 22
Figure 19 Passive Bouncer: A) Circuit; B) Waveforms ...................................................................... 24
Figure 20 Transformer based modulator equipped with two-winding inductor bouncer ...................... 25
Figure 21 CERN LINAC4 Active Bouncer Prototype ........................................................................ 26
Figure 22 Vernier cell in a Marx modulator ....................................................................................... 27
Figure 23 Marx cells equipped with buck regulator ........................................................................... 28
Figure 24 Marx modulator equipped with an inductance capacitor type filter cell ......................... 29
Figure 25 Series connection of a Diode and a SCR bridge for constant power consumption ............ 30
Figure 26 Hybrid power supply ........................................................................................................ 32
Figure 27 Modulator capacitor bank evolution over time ................................................................... 32
Figure 28 a) 2-Phase interleaved H-bridges; b) 2-Phase interleaved buck converter ......................... 34
Figure 29 Undamped LC filter (blue) and critically damped filter (red) .............................................. 36
Figure 30 Multiphase buck converter (3-phases) equipped with an active clamp circuit .................. 37
Figure 31 Multiphase buck with an additional Linear Output Stage .................................................. 38
Figure 32 Output voltage harmonics: a) $f_p<f_s/2$; b) $f_p=f_s/2$; c) $f_p<f_s$ ............................. 40
Figure 33 PWM zero-error bin ........................................................................................................... 41
Figure 34 Ripple reduction obtained by modifying the phase order in a 4-phase interleaved buck converter ................................................................................................................................... 42
Figure 35 Classical monolithic modulator topology .......................................................................... 46
Figure 36 Capacitor charger control strategies .................................................................................. 46
Figure 37 DPAB topology .................................................................................................................. 47
Figure 110 Modulator waveforms during the pulse, charger under constant current control
............................................................................................................................................ 135
Figure 111 Modulator waveforms during several cycles, charger under constant current control
.............................................................................................................................................. 136
Figure 112 Waveforms of the modulator equipped with FVC prototype during the pulse
(charger under constant current control)..................................................................................... 137
Figure 113 Waveforms of the modulator equipped with FVC prototype during several
cycles (charger under constant current control)......................................................................... 138
Figure 114 Active Bouncer prototype with LS and HCS schematic ........................................... 139
Figure 115 MOSFETs driver ..................................................................................................... 140
Figure 116 Linear stage current control with Error Amplifier .................................................... 141
Figure 117 Linear stage double step response ........................................................................... 142
Figure 118 Reduced Scale Modulator prototype equipped with proposed Active Bouncer
topology ...................................................................................................................................... 143
Figure 119 Linear Stage (LS) power converter ....................................................................... 144
Figure 120 High Current Stage (HCS) power stack ................................................................. 144
Figure 121 Output voltage pulse, primary current, main capacitor voltage and Active
Bouncer filter output voltage produced by the modulator prototype equipped with the
SPDC topology ......................................................................................................................... 146
Figure 122 Zoom on the output voltage pulse produced by the modulator prototype
equipped with the SPDC topology.......................................................................................... 147
Figure 123 $V_P$, $V_{AB}$, $V_{bouncer}$, $I_{HCS}$, $I_{LS}$, and $V_{GATE}$ waveforms during a pulse........ 149
Figure 124 $S_h$, $V_P$, $I_1$, $I_2$, $I_3$, $V_{bouncer}$, $S_{SC}$, and $I_{SC}$ waveforms during a pulse .... 150
Figure 125 $V_P$, $V_{bouncer}$, $S_R$, and $I_{SR}$ before and after a modulator prototype pulse .... 151
Figure 126 $V_P$, $V_{Rd}$, and $I_{demag}$ resistor $R_d$ after a modulator prototype pulse ............... 152
Figure 127 $V_{bouncer}$, $I_{HCS}$, and $I_{Rec}$ after a modulator prototype pulse .......................... 153
Figure 128 Modulator load $R_d$ made of several parallel connected Arcol HS300 resistors.
................................................................................................................................................ 154
Figure 129 Reset IGBT switch $S_R$ and two parallel connected resistors $R_R$ ..................... 154
Figure 130 Recovery diode $D_I$ mounted on a heat sink together with a spare diode........ 155
Figure 131 Custom made inductance $L_k$ used to simulate the transformer windings leakage
inductance ................................................................................................................................ 155
Figure 132 Oscilloscope with the following waveforms: $V_P$ in yellow; $I_{LS}$ in blue; $I_P$ in
purple; and $V_{bouncer}$ in green ............................................................................................... 156
Figure 133 SimpowerSystems Matlab Simulink Simulation model of the reduced-scale
modulator prototype equipped with the SPDC topology ........................................................ 157
Figure 134 Simulated waveforms of the modulator prototype equipped with SPDC during a
pulse: Zoom on the output voltage pulse $V_P$; voltage on the main capacitor bank $V_{CAP}$;
active bouncer output filter voltage $V_{bouncer}$; $I_{HCS}$; and $I_{LS}$ ........................................ 159
Figure 135 Klystron modulator design optimization phases ...................................................... 161
Figure 136 Pulse transformer equivalent circuit ....................................................................... 162
Figure 137 Objective function evaluation ............................................................................... 164
Figure 138 Nonlinear inequality constraints evaluation ........................................................... 166
Figure 139 Energy stored in $C_{main}$ and size of $C_{main}$ as a function of its voltage droop
during the pulse ........................................................................................................................ 168
Figure 140 Energy stored in $C_{main}$ and Active Bouncer as a function of its voltage droop
during the pulse ........................................................................................................................ 168
Figure 141 Total Volume - Volume optimization .............................................................. 169
Figure 142 Total volume - Price optimization............................................................... 169
Figure 143 Total volume - Efficiency optimization ....................................................... 170
Figure 144 PFS efficiency - Volume optimization ....................................................... 171
Figure 145 PFS efficiency - Price optimization ......................................................... 171
Figure 146 PFS efficiency - Efficiency optimization .................................................... 172
Figure 147 Total cost - Volume Optimization ............................................................... 173
Figure 148 Total cost - Price optimization ................................................................. 174
Figure 149 Total cost - Efficiency optimization ......................................................... 174
Figure 150 Operating cost for 20 years - Volume Optimization .................................... 175
Figure 151 Operating cost for 20 years - Price optimization ....................................... 176
Figure 152 Operating cost 20 years operation - Efficiency optimization ..................... 176
Figure 153 Optimum switching frequency - Volume optimization .............................. 177
Figure 154 Optimum switching frequency - Price optimization ............................... 178
Figure 155 Optimum switching frequency - Efficiency optimization .......................... 178
Figure 156 Optimum number of phases - volume optimization ................................. 179
Figure 157 Optimum number of phases - Price optimization ..................................... 180
Figure 158 Optimum number of phases - Efficiency optimization .............................. 180
Figure 159 Total volume - Global optimization ......................................................... 182
Figure 160 PFS efficiency - Global optimization ....................................................... 182
Figure 161 Total cost - Global optimization ............................................................... 183
Figure 162 Operating cost for 20 years - Global optimization .................................... 183
Figure 163 Optimum number of phases - Global optimization .................................. 184
Figure 164 Sum of initial modulator cost and operational costs during 20 years - Global Optimization ................................................................. 185
Figure 165 Total volume - Discrete Global optimization .......................................... 186
Figure 166 PFS efficiency - Discrete Global optimization ......................................... 187
Figure 167 Total price - Discrete Global optimization ................................................ 187
Figure 168 Operating cost during 20 years - Discrete Global optimization ................. 188
Figure 169 Initial and operating cost for 20 years - Discrete Global optimization ......... 189
Figure 170 Volume - 1200V Discrete Global optimization ...................................... 190
Figure 171 PFS efficiency - 1200V Discrete Global optimization .............................. 190
Figure 172 Total price - 1200V Discrete Global optimization .................................... 191
Figure 173 Operating cost 20 years - 1200V Discrete global optimization ................... 191
Figure 174 Total cost (initial + 20 years operation) - 1200V Discrete global optimization ................................................................. 192
Figure 175 Optimal Active Bouncer simulation model .............................................. 193
Figure 176 Optimal analytical Active Bouncer waveforms: output voltage pulse, primary current, main capacitor bank voltage, and active bouncer output voltage ............. 194
Figure 177 Optimal analytical active bouncer: Zoom on output voltage pulse flat-top .... 195
Figure 178 Evolution of the correction factor during 10 numerical simulation iterations 196
Figure 179 Evolution of the analytical model error in percentage during 10 numerical simulation iterations ................................................................. 196
Figure 180 Final optimal Active Bouncer waveforms: output voltage pulse, primary current, main capacitor bank voltage, and active bouncer output voltage ............. 198
Figure 181 Final optimal Active Bouncer waveforms: output voltage pulse, active bouncer output voltage, current on HCS phase 1, current on HCS phase 2, and current on linear stage. 

Figure 182 Linear stage thermal simulation model 

Figure 183 Linear stage MOSFETs junction temperature swing during operation 

Figure 184 Final optimal active bouncer: Zoom on output voltage pulse flat-top 

Figure 185 FVC Volume - Global Optimization 

Figure 186 FVC Efficiency - Global Optimization 

Figure 187 Total FVC price - Global Optimization 

Figure 188 FVC operating cost 20 years operation - Global Optimization 

Figure 189 Sum of initial and operating cost for 20 years - Global optimization 

Figure 190 Optimal FVC simulation model 

Figure 191 Optimal analytical FVC waveforms: charging voltage, main capacitor bank $C_{main}$ voltage, FVC output voltage, and FVC output current 

Figure 192 Optimal analytical FVC: Zoom on charging voltage during pulse 

Figure 193 Evolution of FVC correction factor during 10 numerical simulation iterations 

Figure 194 Evolution of FVC analytical model error in percentage during 10 numerical simulation iterations 

Figure 195 Final optimal FVC waveforms: charging voltage, primary current, main capacitor bank voltage, FVC output voltage, and FVC output current 

Figure 196 Final optimal FVC: Zoom on charging voltage during a pulse discharge 

Figure 197 Inductor topological structure and geometrical variables 

Figure 198 Equivalent magnetic circuit of the inductance. A) Complete circuit; B) Simplified circuit
List of tables

Table 1 CLIC klystron modulators specifications ................................................................. 7
Table 2 DPAB, pulse transformer and klystron equivalent circuit simulation parameters .... 55
Table 3 Fixed modulator parameters .................................................................................. 70
Table 4 Optimal Parameters for the three active bouncer topology candidates .............. 71
Table 5 Active Bouncer topologies comparison .................................................................. 75
Table 6 Infineon IGBT module FZ2400R17HP4_B9 Parameters ........................................ 76
Table 7 Infineon IGBT module BSM-200-GB-170-DLC parameters ............................... 76
Table 8 DPAB and SPDC topologies average losses ............................................................ 76
Table 9 Reduced-scale modulator prototype parameters ................................................. 130
Table 10 Active Bouncer prototype passive component values ....................................... 140
Table 11 Active Bouncer power electronics components ................................................. 140
Table 12 Pulse transformer equivalent circuit parameters ................................................ 162
Table 13 Modulator and SPDC Active Bouncer Design Optimization Variables ............ 163
Table 14 Final Optimal CLIC Modulator and SPDC Active Bouncer design parameters 197
Table 15 FVC Design Optimization Variables .................................................................... 202
Table 16 Final Optimal FVC design parameters ............................................................... 211
Table 17 Active bouncer HCS inductance parameters ...................................................... 229
Table 18 Temperature on HCS optimal inductance ......................................................... 230
Table 19 Pulse forming system efficiencies ....................................................................... 231
List of symbols and abbreviations

<table>
<thead>
<tr>
<th>Symbols</th>
<th>Description</th>
</tr>
</thead>
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<tr>
<td>$A_{on}$</td>
<td>Power switch turn-on energy model first order term</td>
</tr>
<tr>
<td>$A_{off}$</td>
<td>Power switch turn-off energy model first order term</td>
</tr>
<tr>
<td>$B_{max}$</td>
<td>Maximum magnetic field density</td>
</tr>
<tr>
<td>$B_{on}$</td>
<td>Power switch turn-on energy model second order term</td>
</tr>
<tr>
<td>$B_{off}$</td>
<td>Power switch turn-off energy model second order term</td>
</tr>
<tr>
<td>$C'_{11}$</td>
<td>Transformer primary capacitance referred to the primary side</td>
</tr>
<tr>
<td>$C'_{22}$</td>
<td>Transformer secondary capacitance referred to the primary side</td>
</tr>
<tr>
<td>$C_{bouncer}$</td>
<td>Active bouncer capacitor bank</td>
</tr>
<tr>
<td>$C_{main}$</td>
<td>Modulator main capacitor bank</td>
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<tr>
<td>$C_{FVC}$</td>
<td>Fast Voltage Compensator output filter capacitor</td>
</tr>
<tr>
<td>$C_{HS}$</td>
<td>Heat-sink thermal capacitance</td>
</tr>
<tr>
<td>$C_{p}$</td>
<td>Specific heat of air</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>$E_{a}$</td>
<td>Activation energy</td>
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<tr>
<td>$E_{ideal_pulse}$</td>
<td>Energy released during an ideal output voltage pulse</td>
</tr>
<tr>
<td>$E_{on}$</td>
<td>Power switch datasheet turn-on energy</td>
</tr>
<tr>
<td>$E_{off}$</td>
<td>Power switch datasheet turn-off energy</td>
</tr>
<tr>
<td>$E_{real_pulse}$</td>
<td>Energy released during a real output voltage pulse</td>
</tr>
<tr>
<td>$E_{rr}$</td>
<td>Diode reverse recovery energy</td>
</tr>
<tr>
<td>$F$</td>
<td>Farad</td>
</tr>
<tr>
<td>$FBSOA$</td>
<td>Forward bias safe operating area</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>Maximum switching frequency</td>
</tr>
<tr>
<td>$f_{min}$</td>
<td>Minimum switching frequency</td>
</tr>
<tr>
<td>$f_{s}$</td>
<td>Switching frequency</td>
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</tbody>
</table>
\( f_p \) Perturbation frequency
\( H \) Henry
\( H_{Al} \) Aluminum heat capacitance
\( H_{bp} \) Heat-sink base plate height
\( h_{conv} \) Heat exchange coefficient
\( H_f \) Heat-sink fin height
\( I_{CH} \) Capacitor charger current
\( I_c \) Power switch collector current
\( I_F \) Diode forward current
\( I_{FVC} \) Fast Voltage Compensator output current
\( I_{kly} \) Klystron current
\( I_{kn} \) Nominal output pulse current
\( I_L \) Active bouncer output current
\( I_P \) Pulse transformer primary current
\( I_{rr} \) Diode reverse recovery current
\( J \) Current density
\( J_{RMS} \) RMS current density
\( k_{Air} \) Thermal conductivity of air
\( k_{Al} \) Thermal conductivity of aluminum
\( k_{B} \) Boltzmann constant
\( k_c \) Optimization analytic models correction factor
\( k_f \) Power switch conduction losses current scaling factor
\( k_{Rg,on} \) Power switch losses model turn-on gate resistance scaling factor
\( k_{Rg,off} \) Power switch losses model turn-off gate resistance scaling factor
\( k_{rr} \) Diode reverse recovery losses scaling factor
\( k_{Vce,on} \) Power switch losses model turn-on voltage scaling factor
\( k_{Vce,off} \) Power switch losses model turn-off voltage scaling factor
\( L_B \) Active bouncer equivalent output filter inductor
\( L_{calc} \) Analytic inductor value
\( L_k \) Transformer leakage inductance
\( L_m \) Transformer magnetizing inductance
\( L_{\text{mag}} \)  
Magnetic circuit length

\( L_t \)  
Heat-sink total length

\( M_{\text{core}} \)  
Magnetic core mass

\( \text{MLT} \)  
Mean length per turn

\( N \)  
Number of turns

\( N_{\text{cf}} \)  
Power switch number of thermal cycles to failure

\( N_f \)  
Heat-sink number of fins

\( N_{\text{phases}} \)  
Number of phases

\( N_u \)  
Nusselt number

\( \eta_{\text{ch}} \)  
Capacitor charger electrical efficiency

\( \eta_{\text{mod \_global}} \)  
Modulator global electrical efficiency

\( \eta_{\text{pfs}} \)  
Pulse forming system electrical efficiency

\( \eta_{\text{pulse}} \)  
Pulse electrical efficiency

\( P \)  
Power

\( P_{\text{average}} \)  
Average power

\( P_{\text{ch}} \)  
Capacitor charger peak power

\( P_{\text{cond}} \)  
Power switch conduction losses

\( P_{\text{cond \_diode}} \)  
Diode conduction losses

\( P_{\text{drive}} \)  
Semiconductor driving losses

\( P_{\text{HCS}} \)  
Active Bouncer High Current Stage losses

\( P_{\text{LL}} \)  
Linear operation losses

\( P_{\text{mag}} \)  
Inductor magnetic losses

\( P_{\text{mod \_out}} \)  
Output pulse peak power

\( P_{\text{PFS \_in}} \)  
Pulse forming system peak power

\( Pr \)  
Prandtl number

\( \text{Price}_{\text{cap}} \)  
Capacitor price

\( \text{Price}_{\text{ind}} \)  
Inductor price

\( P_{\text{rr}} \)  
Diode reverse recovery losses

\( P_{\text{SLL}} \)  
Semiconductor linear losses

\( P_{\text{sw}} \)  
Power switch switching losses

\( Q_{\text{rr}} \)  
Diode reverse recovery charge
$R_1$ Transformer primary winding resistance
$R_2'$ Transformer secondary winding resistance referred to the primary side
$R_{bp}$ Heat-sink base plate thermal resistance
$R_D$ Diode forward voltage model equivalent series resistance
$Re^*$ Reynolds modified number
$Rt$ Power switch forward voltage model equivalent series resistance
$
\mathcal{R}$ Reluctance
$\mathcal{R}_{cc}$ Magnetic core central column reluctance
$\mathcal{R}_{ec}$ Magnetic core external column reluctance
$\mathcal{R}_{gcc}$ Magnetic core central column air-gap reluctance
$\mathcal{R}_{ec}$ Magnetic core external column air-gap reluctance
$\mathcal{R}_{tot}$ Total equivalent reluctance of a magnetic circuit
$T$ Temperature
$T_{Amb}$ Ambient temperature
$T_{Core,Ext}$ Temperature on magnetic core surface
$T_{Cu,Ext}$ Temperature on copper core surface
$T_{Cu}$ Temperature on internal copper coils layers
$T_{sw}$ Switching frequency period
$t_{Cu,\text{max}}$ Maximum temperature in the copper
$t_{\text{fall}}$ Output voltage pulse falling-time
$t_{\text{flat}}$ Output voltage pulse flat-top time
$t_{\text{on}}$ Power switch turn-on time
$t_r$ Pulse transformer turns ratio
$t_{\text{rise}}$ Output voltage pulse rise-time
$t_{rr}$ Diode reverse recovery time
$t_{\text{set}}$ Output voltage pulse settling time
$t_{\text{trig,init}}$ Time required to initialize the current in the active bouncer output filter inductances
$V_{AB}$ Active bouncer capacitor bank voltage
$V_{Air}$ Air speed
$V_{b,\text{max}}$ Maximum output voltage value the active bouncer can deliver
$V_{CE}$ Power switch collector-emitter voltage during the blocking state
$V_{CE,o}$ Power switch forward voltage model equivalent DC voltage
\( V_{\text{CE,sat}} \)  Power switch saturation voltage
\( V_{\text{CH}} \)  Modulator capacitor charger output voltage
\( V_{\text{Cmain}} \)  Voltage across the modulator main capacitor bank
\( V_{\text{Cu}} \)  Inductor copper volume
\( V_{\text{F}} \)  Diode forward voltage
\( V_{\text{FO}} \)  Diode forward voltage model equivalent DC voltage
\( V_{\text{FVC}} \)  Fast Voltage Compensator output voltage
\( V_{\text{HS}} \)  Heat-sink total volume
\( V_{\text{Kly}} \)  Klystron voltage
\( V_{\text{mag,total}} \)  Total magnetic core volume
\( V_{\text{Cu}} \)  Inductor copper volume
\( V_{\text{P}} \)  Pulse transformer primary voltage
\( V_{\text{OVS}} \)  Output voltage pulse overshoot
\( W_{\text{cap}} \)  Energy stored in capacitors
\( W_{\text{f}} \)  Heat-sink fin width
\( W_{\text{if}} \)  Heat-sink distance between fins
\( W_{\text{mag}} \)  Magnetic energy stored in an inductor
\( W_{\text{t}} \)  Heat-sink total width
\( Z_{\text{th}} \)  Thermal impedance
\( Z_{\text{th,jc}} \)  Junction-case thermal impedance
\( \alpha \)  Optimization correction smoothing factor
\( \Delta B \)  Magnetic density swing
\( \Delta V \)  Modulator main capacitor bank voltage discharge during the pulse
\( \Delta T_{\text{j}} \)  Power switch junction thermal swing
\( \Omega \)  Ohm
\( \phi \)  Magnetic flux
\( p \)  Klystron perveance
\( \rho \)  Resistivity
\( \rho_{\text{air}} \)  Air density
\( \rho_{\text{N}} \)  Aluminum density
\( \rho_{\text{Cu}} \)  Copper resistivity
\( \rho_{\text{mlm}} \) Magnetic loss mass density
\( \rho_{\text{mlv}} \) Magnetic loss volumetric density
\( \mu_{\text{air}} \) Air dynamic viscosity

**Abbreviations**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analogue to Digital Converter</td>
</tr>
<tr>
<td>ALAG</td>
<td>Augmented Lagrangian</td>
</tr>
<tr>
<td>CERN</td>
<td>European Organization for Nuclear Research</td>
</tr>
<tr>
<td>CLIC</td>
<td>Compact Linear Collider</td>
</tr>
<tr>
<td>DB</td>
<td>Drive Beam</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DPAB</td>
<td>Dual Purpose Active Bouncer</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent series resistance</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent series inductance</td>
</tr>
<tr>
<td>FTS</td>
<td>Flat-top pulse voltage stability</td>
</tr>
<tr>
<td>GAs</td>
<td>Genetic algorithms</td>
</tr>
<tr>
<td>HCS</td>
<td>High Current Stage</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>ICFA</td>
<td>International Committee for Future Accelerators</td>
</tr>
<tr>
<td>iGSE</td>
<td>Improved Generalized Steinmetz Equation</td>
</tr>
<tr>
<td>ILC</td>
<td>International Linear Collider</td>
</tr>
<tr>
<td>LEEPCI</td>
<td>Laboratoire d’Électrotechnique, d’Électronique de Puissance et de Commande Industrielle</td>
</tr>
<tr>
<td>LHC</td>
<td>Large Hadron Collider</td>
</tr>
<tr>
<td>LINAC</td>
<td>Linear Accelerator</td>
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<tr>
<td>LLRF</td>
<td>Low level RF</td>
</tr>
<tr>
<td>LS</td>
<td>Linear Stage</td>
</tr>
<tr>
<td>LTI</td>
<td>Linear Time-Invariant</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MSPS</td>
<td>Mega samples per second</td>
</tr>
<tr>
<td>MTBF</td>
<td>Mean time between failures</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>PETS</td>
<td>Power Extraction and Transfer Structures</td>
</tr>
<tr>
<td>PFS</td>
<td>Pulse Forming System</td>
</tr>
<tr>
<td>ppm</td>
<td>Parts per million</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>REPR</td>
<td>Repetition rate</td>
</tr>
<tr>
<td>SPDC</td>
<td>Split Power and Droop Compensator</td>
</tr>
<tr>
<td>SQP</td>
<td>Sequential quadratic programming</td>
</tr>
<tr>
<td>QSW</td>
<td>Quasi-square-wave topology</td>
</tr>
</tbody>
</table>
True heroism consists in turning dreams into realities and ideas into deeds.

Alfonso Daniel Rodríguez Castelao
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CHAPTER 1

1 INTRODUCTION

Pulsed power converters are widely used in an extensive range of civil and military applications, particularly in the field of medical and physics research. Their utilization is also becoming very important in industrial applications, where the advent of new power electronics technologies is increasing their attractiveness. This kind of power converters slowly accumulate energy and release it during short periods of time, ideally producing square-shaped voltage or current intense pulses at high power levels. Their operation principle is based on the controlled discharge of an initially pre-charged capacitor bank using different configurations of DC-DC converters, usually named pulse forming systems (PFS). In comparison with common DC power converters, the main benefit pulsed power converters hold is a drastic reduction of the losses, a certain degree of decoupling from the utility grid (total peak power delivered to the load not seen by the grid), reduced size and cost.

Typical pulsed power converters like Marx Generators, Pulse Forming Networks, Multi-stage Blumlein Lines or Magnetic Pulse Compressors, conventionally used magnetic and gas based switches, such as spark gaps and thyatrons, mainly due to their high voltage and high current switching capabilities. However, these switches present serious drawbacks like short life-cycle, low operational frequency, big size, high cost, low efficiency and reliability. Nowadays, solid-state switches (SCRs, IGBTs and IGBT stacks) are becoming the preferred technology. They present as main benefits: higher efficiency, high switching frequency operation, extended life cycles, compact size and high reliability. On the other hand, their voltage ratings are still relatively low and, therefore, the topologies of pulsed power converters and their associated control methods present many challenges and are evolving in order to use this technology in medium and high voltage applications. Being relatively new, there is a lack of literature and industrial expertise in this domain.

The new generation of pulsed power converters is demanding an extremely high level of performance never reached before in terms of large signal bandwidth, low ripple and efficiency. Typical specifications coming from new linear accelerators are: very accurate pulse flat-top precision, rise and stabilization times of just a few μs, and ripple levels below 100ppm for peak power levels in the MW range. This is the case of the klystron modulators required for a new linear accelerator under study at CERN, The Compact Linear Collider (CLIC), whose operating principle will be introduced hereafter.
1.1 Framework

The particle physics community, and particularly the International Committee for Future Accelerators (ICFA), has decided that the results from the Large Hadron Collider (LHC), currently running at CERN, will need to be complemented by experiments at a lepton collider. Two different accelerators are being explored as candidates at different energy levels: the International Linear Collider (ILC), aiming for an e+e− collider with an energy of 500 GeV, and CLIC, also an e+e− collider but with a center-of-mass collision energy of 3 TeV and a luminosity of $2.10^{34}$ cm$^{-2}$s$^{-1}$.

CLIC is based on a novel acceleration scheme, which allows reaching an accelerating gradient of ~100 MV/m in an efficient and compact accelerator complex. An equivalent classic LINAC accelerator would require a large number of klystrons (~35000 of 50 MW each considering a pulse compression equal to a factor 5) to be confined in a maximum length of 50 Km, implying higher cost and lower efficiency. This new scheme is based on the generation of a "Drive Beam", its compression and reconversion into RF power close to the Main Beam accelerating structures. Figure 1 shows the layout of the CLIC accelerator complex. The "Drive Beam" is generated in two main LINACs and time compressed using delay loops and combiner rings, before being decelerated in special RF structures (PETS) in order to generate the necessary RF power for accelerating the main beam. This two-beam acceleration scheme offers good power efficiency (mainly because the transport of power to the place where it is converted to RF is performed using a nearly lossless electron beam).

![Figure 1 Layout of the Compact Linear Collider (CLIC)](image-url)
A total of 1638 modulators of 24MW peak power each will be required for powering the klystrons in the "Drive Beam". These modulators will be synchronously operated with a repetition rate of 50 Hz. With this operating mode, a total pulsed peak power of 39.312 GW must be produced, as illustrated in Figure 2, equivalent to 294.84 MW of average power consumption only. The total available power for the whole complex at the grid connection point is 400 MW, and exceeding this limit would compromise the feasibility of the project due to the enormous cost increase. In addition, the utility grid can tolerate only a few percent of this power fluctuation (difference between the total pulsed peak power produced and the total average power consumption) and, thus, the klystron modulators system must be designed such that only a constant power (294.84 MW) is withdrawn from the AC network. Moreover, the tolerances in the RF quality (directly linked to the modulator pulse specifications) are extremely tight: 0.2% for the RF power and 0.05º for the RF phase. These tolerances are translated in very challenging output voltage pulse specifications for the modulator in terms of flat-top stability (0.85% for an output voltage pulse of 150kV) and repeatability (100 ppm). Considering the important amount of modulators required and the total power consumption value, the overall efficiency has to be maximized in order to confine the overall power consumption within an acceptable range.

**Figure 2** Total output pulsed power delivered by CLIC klystron modulators synchronous operation
In order to carry out the feasibility study of such a klystron modulator, CERN organized an international collaboration with different institutions, as shown on Figure 3. The common challenges were studied directly by CERN, Nottingham University studied the CLIC grid layout, and two Universities studied two different klystron modulators topologies. The split-core transformer based topology was studied by ETH Zurich, and the monolithic transformer based topology was studied by the LEEPCI Laboratory at Laval University. The work package at Laval University was split into two different doctoral thesis, the one focused on the design of the monolithic pulse transformer, and a second one based on the design of the droop and power compensators for the modulator, which concerns the present PhD dissertation.

![Figure 3 CLIC Drive-Beam Klystron Modulators International Collaboration](image)

1.2 Project needs

In addition to the constant power consumption requirement, the efficiency of each modulator and klystron has to be maximized to guarantee the feasibility of the whole project. In order to understand the global efficiency of a klystron modulator, several efficiency definitions have to be first introduced.

A klystron modulator is generally composed of:

- A capacitor charger, which performs AC-DC conversion and charges an intermediate energy storage capacitor.
• A pulse forming system (PFS), which performs the task of creating the output voltage pulse using the energy stored in the intermediate energy storage capacitor.

Figure 4 presents the simplified structure of a klystron modulator.

![Figure 4 Klystron Modulator block diagram](image)

We can define the capacitor charger efficiency as the ratio between the power delivered to the capacitor bank by the charger, and the power taken from the utility grid:

$$\eta_{ch} = \frac{P_{ch}}{P_{grid}}$$  \hspace{1cm} (1)$$

In a similar way, we can define the PFS efficiency as the ratio between the power delivered to the klystron by the PFS and the power withdrawn from the capacitor bank:

$$\eta_{PFS} = \frac{P_{mod\_out}}{P_{PFS\_in}}$$  \hspace{1cm} (2)$$

In order to have a complete picture of the global modulator efficiency, we also have to define the pulse efficiency, whose magnitude tells us how similar the effective real pulse is from an ideal square shaped pulse. It is defined as the ratio between the energy delivered during a real pulse and the energy delivered considering an ideal pulse [1]:

We can define the capacitor charger efficiency as the ratio between the power delivered to the capacitor bank by the charger, and the power taken from the utility grid:
This concept is illustrated in Figure 5, where we can see that many pulse parameters have an impact on the pulse efficiency: the rise time $t_{\text{rise}}$ (time to reach $V_{\text{kn}}$); the fall time $t_{\text{fall}}$ (time to abandon the flat-top and decrease to 0 V); the voltage overshoot $V_{\text{OVS}}$; the settling time $t_{\text{set}}$; and the flat-top stability (difference between the maximum and minimum voltage values during the flat-top $t_{\text{flat}}$).

![Figure 5 Performances definitions of the modulator output voltage pulse](image)

The global efficiency of the modulator can, therefore, be defined as:

$$\eta_{\text{mod, global}} = \eta_{\text{pulse}} \eta_{\text{PSF}} \eta_{\text{ch}}$$  \hspace{1cm} (4)

From the challenging CLIC efficiency and RF quality requirements, CERN has established the pulse specifications and modulator efficiencies that the final modulator has to achieve [1]. These specifications are shown in Table 1.
We can notice the tight dynamical specifications of 3 µs for rise and fall times; the high efficiencies required in order to minimize the grid power consumption; and the challenging output voltage pulse performances of 0.85% flat-top stability and 1% overshoot.

These challenging specifications exceed state-of-the-art solutions, particularly because of the extremely stable output voltage pulse required. A klystron modulator based on a monolithic transformer topology achieving these specifications has never been designed; therefore new droop compensation systems, optimized pulse transformers, and power compensators have to be designed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal pulse voltage</td>
<td>$V_{kn}$</td>
<td>150 kV</td>
</tr>
<tr>
<td>Nominal pulse current</td>
<td>$I_{kn}$</td>
<td>160 A</td>
</tr>
<tr>
<td>Pulse peak power</td>
<td>$P_{mod_out}$</td>
<td>24 MW</td>
</tr>
<tr>
<td>Rise &amp; fall times</td>
<td>$t_{\text{rise}}, t_{\text{fall}}$</td>
<td>3 µs</td>
</tr>
<tr>
<td>Settling time</td>
<td>$t_{\text{set}}$</td>
<td>5 µs</td>
</tr>
<tr>
<td>Flat-top length</td>
<td>$t_{\text{flat}}$</td>
<td>140 µs</td>
</tr>
<tr>
<td>Repetition rate</td>
<td>REPR</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Voltage overshoot</td>
<td>$V_{\text{ovs}}$</td>
<td>1 %</td>
</tr>
<tr>
<td>Flat-top stability</td>
<td>FTS</td>
<td>0.85 %</td>
</tr>
<tr>
<td>Charger electrical efficiency</td>
<td>$\eta_{\text{ch}}$</td>
<td>96 %</td>
</tr>
<tr>
<td>PFS electrical efficiency</td>
<td>$\eta_{\text{pfs}}$</td>
<td>98 %</td>
</tr>
<tr>
<td>Pulse efficiency</td>
<td>$\eta_{\text{pulse}}$</td>
<td>95 %</td>
</tr>
<tr>
<td>Modulator global efficiency</td>
<td>$\eta_{\text{mod_global}}$</td>
<td>89.3 %</td>
</tr>
</tbody>
</table>
1.3 PhD Objectives

The main objective of the PhD consists in the study and design of power electronics solutions to be optimally integrated in a klystron modulator based on a monolithic pulse transformer, with the following two important requirements: the modulator must operate at constant power consumption from the grid, and must respect the CLIC challenging specifications in terms of output pulse quality and efficiency. The peculiarity of this work consists in developing a global or integrated design methodology, which includes all the modulator sub-components (capacitor charger, capacitor bank and pulse transformer). The PhD aims to design and construct a reduced scale prototype to validate the topological choices and the design methodology, and to propose an optimal dimensioning of the final full-scale CLIC modulator to be tested at CERN.

Due to the challenging pulse specifications required from the modulator and, accordingly, from the PFS, the study will address the main research topics concerning pulsed power converters design (high bandwidth, efficiency and low ripple) at levels that go beyond the current state of the art. The manifold research topics will include topological innovations and improvements in the control solutions. The study will also provide general hints regarding the most suitable topologies for future high performance pulsed power converters, whose applications could be extended to various industrial applications.

The objectives and contributions of this PhD can be summarized in the following:

- Study, design and experimental validation of a droop compensation system topology able to achieve CLIC challenging output pulse specifications. Due to the reduced pulse width and required precision, this system must be active and also be able to withstand all the modulator primary current (>2 kA). Efficiency must be optimized to respect the modulator global efficiency requirement. The final topology must be validated experimentally using reduced scale prototypes.

- Study, design and experimental validation of a power compensation system able to make a klystron modulator based on a monolithic pulse transformer operate at constant power consumption from the utility grid. Because this compensation system must be active, efficiency must be maximized. The intermediate energy storage should be reduced as much as possible by increasing the power converter bandwidth, in order to reduce the total space required (which has a direct impact on civil engineering costs) and for safety purposes (total energy stored). The final power compensator also has to be validated experimentally with a reduced scale prototype integrated into a klystron modulator.
• Develop a general and versatile global optimization design tool composed of analytical design models able to accurately predict the performances of the different modulator subcomponents. This tool allows to understand the different design trade-offs, the quick evaluation of changes on load and input specifications\(^1\), and the final optimal design of the CLIC klystron modulator.

• Optimal design of a full-scale klystron modulator for CLIC able to produce 29MW pulses (180 kV and 161 A; or 150kV and 193A) with a repetition rate of 50Hz respecting all CLIC specifications.

The adopted methodology to achieve all these objectives is detailed in the different chapters of this thesis. After this introduction, chapter 2 presents the state of the art of klystron modulators, droop compensators, power compensators, and high-bandwidth low ripple power converters. Chapter 3 presents the topological study of different power converter structures to fulfill the droop and power compensation functions. Two new topologies fulfilling the specifications are identified, and one of them is selected, following a detailed comparison and performances evaluation based on numerical simulation results. Chapter 4 presents a general overview of the modulator optimal design methodology, the design method detail description, and the research work proposed planning. Chapter 5 presents all the analytical design models developed to accurately predict semiconductor losses; and the thermal behavior, volume, and cost of each compensator subcomponent. Chapter 6 presents the constructed power and droop compensators reduced scale prototypes, and their detailed experimental validation results. Chapter 7 details the optimal design of the full power droop and power compensators for CLIC klystron modulator, following the design methodology previously presented in Chapter 4. Finally, the last chapter presents the research work conclusions and the future works.

\(^1\) In parallel to this research work, the klystron tube was being designed and developed, and different CLIC grid scenarios explored; the impact of different load and primary voltage changes had to be quickly evaluated and understood.
CHAPTER II

2 STATE OF THE ART

This chapter provides a literature review of the different klystron modulator topologies, voltage droop regulators and design solutions to achieve high bandwidth and low ripple power converter designs.

2.1 Klystron Modulators

Klystron modulators are typically classified depending on their pulse length. Hence, modulators producing pulses of more or less than 100\(\mu\)s\(^2\) are designated as "Long pulse modulators" or "Short pulse modulators", respectively. A different taxonomy also classifies them in "transformer-less" and "transformer-based" modulators, due to the common utilization of this device. However, these classifications are based on the modulator ratings / voltage-step up method and not on their operation mode. As a consequence, we can find that modulators with the same topology can be classified as "long pulse" or short pulse depending on the dimensioning (i.e. capacitor bank size). To avoid this issue, in this document we consider a classification depending on the controlled or uncontrolled flat-top production method, respectively.

As the klystron modulator under study requires an accurate flat-top production, only modulator topologies with controlled flat-tops will be briefly introduced hereafter to provide an overview of the existing alternatives to the monolithic transformer based modulator topology, concerned by our study.

2.1.1 Polyphase converter modulator

This polyphase resonant converter modulator was developed at Los Alamos National Laboratory (LANL) for the Oak Ridge National Laboratory (ORNL) Spallation Neutron Source [2]. The topology is depicted in Figure 6. Each converter bus voltage is obtained by first stepping down the voltage in a substation cast-resin transformer and then converted to DC using a SCR controlled rectifier.

\(^2\) Some authors consider a value of 50\(\mu\)s
Three H-bridges operating as inverters are used to generate polyphase 20 kHz square voltage waveforms at the primaries of a step-up transformer. Zero voltage switching (ZVS) at turn-on is achieved by tuning the leakage inductance and the overall secondary capacitance of the transformer, minimizing the switching losses. The secondary windings of the transformer are star-connected. The output voltage is finally rectified using a standard six-pulse rectification circuit (using low loss, fast recovery diodes) with a "pi-R" type filter network.

The main advantages of this topology are the inherent voltage droop correction capability and the reduced magnetic energy stored in the high frequency step-up transformer due to the AC 3-phase operation. However, the topology is quite complex and presents an important number of components, which could have an impact on overall cost and reliability.

The ORNL modulator produces pulses of 140 kV, with a pulse width of 1.2 ms and a peak power of 11 MW. Results show a rise time which is about 20 µs and efficiency levels better than 93% at full power [3]. The output voltage pulse precision achieved is better than 0.25% using adaptive control methods [4], while the main capacitor bank experiences a voltage drop of 20%. No results concerning power fluctuation have been published in the literature, although this modulator does not operate at constant power consumption.

2.1.2 ITER Gyrotron modulator

Two high voltage power converters were designed for the International Thermonuclear Experimental Reactor (ITER) Heating and Current Drive Gyrotron [5, 6]. They share the same topology, based on the series connection of elementary power modules, each module with its own DC power supply, as depicted in figures 7 and 8. A multi-secondary transformer is used to adapt the input voltage from the grid to the input voltage required by each elementary power module. A prototype operating at 60 kV and 80 A was installed at the European Electron Cyclotron Test Facility at CRPP (Lausanne, Switzerland) [7], achieving a voltage settling time of 15 µs, shutdown time (required in case of arc in the gyrotron, between cathode and body) of 10 µs, an output voltage
accuracy of 1% and an efficiency of 97%. A new high voltage power converter at higher power ratings (90 kV and 90 A) for the ITER Lower Hybrid Current Drive is still under study [8].

This topology could be considered as an inductive adder. The main advantages are the integrated voltage correction capability and the fact that it does not require the utilization of a pulse transformer. The main drawback would be its reliability: although the system is modular, the modulator cannot continue operating if one of the modules output diode fails. No results concerning power fluctuation have been presented. However, a low impact on the grid, in terms of power factor (0.98) and low harmonic content, has been reported.
2.1.3 MARX modulator

The Marx generator is an electrical circuit first described by Erwin Otto Marx in 1924. The operation of the modulator is based on the slowly charge of capacitors connected in parallel, followed by a discharge where all the capacitors are reconnected in series (initially using spark gaps and gas tubes but, nowadays, using solid-state technology) as a voltage adder [9, 10, 11, 12]. The operation of this modulator topology is illustrated in figure 9.

The Marx modulator experiences a voltage droop due to the capacitors discharge. In order to compensate this phenomenon several voltage droop compensators have been proposed: bouncer circuits [13], Vernier cells [14], buck converters [15, 16]. These compensation methods will be presented in 2.2.

The "Marx P2" developed at the Stanford Linear Accelerator Center (SLAC), produces 120 kV and 140 A pulses of 1.6 ms with a repetition rate of 5 Hz. The achieved output pulse flat-top precision was ±0.5% and the overall efficiency ~95%.

![Figure 9 A) Marx Modulator topology. B) Charging circuit. C) Discharging circuit.](image-url)
The main advantages of this topology are the utilization of low and medium voltage solid-state switches, their compactness, an announced very high efficiency, and the fact that it is oil-free and presents a modular design. However it presents some difficulties concerning air insulation, which is affected by the air conditions and may have an impact in reliability. The control electronics, including the IGBT drivers, can be affected by the fast changing intense electric fields and the high number of switches. These limitations can strongly influence the modulator reliability.

2.1.4 Jema modulator

A Spanish company, Jema, has recently designed a modulator with a topology in between the Marx Modulator and a Hard Switch Modulator [17, 18, 19, 20]. A 1500 kVA input step-down transformer provides the 30 electrical phase-shift required by a 1300 A, 12-pulse thyristor rectifier, which provides a DC bus voltage of 1000 V. Each of a total of 12 inverters, operating at 4 kHz with soft zero-voltage switching (ZVS), is connected to the primary of individual step-up medium-frequency cast resin transformers. Each transformer has 6 secondary windings, which are connected to a diode bridge in order to rectify the AC voltage. Finally, all the modules are connected in series by means of an IGBT at the output of each high voltage output stage. The discharge of the output capacitors during the pulse is corrected by the operation of the 4 kHz inverters. The schematic of the modulator is depicted in figure 10.
A first modulator prototype able to produce 85 kV and 160 A, 1.5 ms pulses at 60 Hz has achieved rise and fall times of 10 µs, low output voltage ripple and output voltage droop. The main advantages of this topology are the modularity, the utilization of standard industrial components, a low output voltage ripple, and the utilization of a dry solution for the transformer (no oil). The designers also claim that it presents high levels of reliability (high MTBF), mainly due to the operation of the inverters at relatively low frequencies (4 kHz). However the topology does not operate at constant power consumption and, in order to produce pulses in the CLIC range (150 kV, 140 µs), the inverters frequency and probably the output stage capacitances should be increased. No results concerning efficiency have been presented yet.

### 2.1.5 Modulator / Switching Buck Regulator

Diversified Technologies Inc. (DTI) and Communication and Power Industries (CPI) developed a new modulator for testing and operate high power microwaves tubes, such as klystrons and gyrotrons [21, 22]. Figure 11 shows the schematic of this topology, which is composed of two different stages. The first one consists of a solid-state switch which is used to modulate in PWM a high voltage from a capacitor bank into an intermediate LC filter (as a buck regulator). The second stage is a simple fast series switch, which transfers the power to the
load during the pulse. The buck regulator stage operates between 4 and 10 kHz using a patented DTI switch technology, which is able to share the load equally between devices (by controlling the switches in their ohmic region during commutations, probably using active gate control). A 140 kV, 500 A modulator (the world’s highest power solid-state high voltage modulator), was developed using this topology and installed at CPI in Palo Alto, California. This modulator is able to produce pulses from 1µs to DC, achieving repetition rates of more than 10 kHz. Results have shown levels of efficiency over 95% with less than 40V peak to peak ripple.

![Modulator/Switching Buck Regulator Topology](image)

The main advantages of this topology are its simplicity, its compactness, and the wide range of pulse width operation. However their switch technology is not an industrial standard and presents some reliability problems in case one of the series connected switches fails. An increase of modularity in order so solve this problem could have a strong impact on modulator cost.

### 2.1.6 Thomson modulator

Thomson & Multimedia has built a novel modulator for the European XFEL project at DESY (Germany) [23, 24]. This modulator is able to produce pulses up to 12 kV and 2 kA with a pulse width of 1.7 ms and a nominal repetition rate of 10 Hz. The modulator is based on the pulse step modulator\(^3\) (PSM) principle [25]. It achieves good pulse flatness and operates at constant power consumption.

The topology is composed of 24 switching modules which can be connected in series or bypassed, as shown in figure 12. The modules are regulated using PSM technology (a particular kind of PWM modulation with a switching frequency of 20 kHz per module, which makes a virtual equivalent switching frequency of 480 kHz).

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\(^3\) Introduced by Thomson, Switzerland (formerly BBC/ABB) in 1983 and based on the series connection of switched mode power supply modules
providing full compensation of the voltage droop on the storage capacitors during the pulse. Four modules are equipped with additional switching modules in order to demagnetize the pulse transformer between pulses and to dissipate the inductive stored energy under klystron arcing conditions. The constant power consumption is achieved by using a boost converter in each power module, which are operated under a constant power control loop.

No concrete results regarding efficiency or power fluctuation have been published yet, though a pulse flatness variation of less than ±0.3% has been reported [26].

2.1.7 Monolithic transformer-based modulator

This topology was originally designed by the Fermi National Accelerator Laboratory (Fermilab) [27, 28] and DESY [29, 30, 31] in 1993 for the TESLA superconducting linear accelerator. It is composed of a medium voltage AC/DC converter which slowly charges a capacitor bank, and a main MV switch which discharges the capacitor.
bank through a step-up pulse transformer, as depicted in figure 13. This capacitor bank is usually dimensioned to experience a voltage droop of 10% to 20% during the pulse, with the purpose of minimizing its size and the total energy stored. A bouncer circuit\(^4\) is used to compensate the voltage droop in the capacitor bank and in the pulse transformer during the pulse. After every pulse, the pulse transformer is demagnetized with an undershoot network.

Several modulators using this topology have been designed and constructed. The first monolithic transformer based modulators used GTO based main switches [32, 33], but they were soon replaced by IGBTs stacks [34] or IGCTs, respectively. DESY has constructed modulators of this type capable of producing 120 kV and 140 A pulses of 1.6 ms with a repetition rate of 10 Hz [35, 36, 37]. They achieved modulator efficiency levels of 86% and a pulse flatness of 1%. At the High Energy Accelerator Research Organization (KEK) they have also constructed a monolithic modulator [38, 39] capable of producing 120 kV and 140 A pulses, but with a pulse width of 1.7 ms, a repetition rate of 5 Hz, and a pulse flatness of 0.5%. Another monolithic transformer-based modulator, shown in figure 14, was designed and constructed at CERN for powering LINAC4 klystrons [40, 41, 42]. This modulator produces 110 kV and 50 A pulses of 1.8 ms with a repetition rate of 2 Hz. They achieved rise and fall times of 150µs, and a pulse flatness better than 1% with no high frequency ripple on flat-top.

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\(^4\) This circuit will be reviewed in detail in 2.2
The main advantages of this topology are its simplicity, the reduced number of components, and the fact that all power electronics components are in a medium voltage stage on the primary side, which make it very reliable. The main drawback is the strong influence of the pulse transformer parasitics on modulator performances, in terms of rise and fall times. The grid interface is usually realized with commercial capacitor chargers that do not operate at constant power consumption.

![Figure 14 CERN LINAC4 monolithic transformer modulator](image)

### 2.1.8 Hard Switch modulator

Diversified Technologies (DTI) has designed a “Hard-Switch” modulator which makes use of their specific multiple switch combination technology [43, 44]. It is composed of a capacitor bank, a HV switch that directly connects the capacitor bank to the load during the pulse, and a bouncer circuit to compensate the voltage drop in the capacitor during the pulse. The design is similar to the monolithic transformer modulator from Fermilab and DESY, but it is using a high voltage switch in the output stage, instead of a medium voltage switch and a step-up transformer. Figure 15 shows a simplified electrical schematic of this topology.
DTI developed a Hard-Switch modulator for the International Linear Collider (ILC), capable of producing 135 kV and 165 A pulses of 1.5 ms with a repetition rate of 5 Hz. The achieved pulse flatness was better than 1%. The designers claim that this modulator topology could be between 30% and 50% less expensive in production than a monolithic transformer-based modulator with the same specifications. However this topology also presents some drawbacks: the high voltage switch based on the DTI patented technology has a direct impact on cost and reliability, because all the components are at high-voltage. The insulation requirements increase the design complexity (an insulated high voltage cabinet is required). Consequently, as for the Marx modulator, insulation requirements imply volume increase.

### 2.1.9 Matrix transformer modulator

In order to overcome the rise time limitation introduced by the utilization of pulse transformers, a new modulator topology based on a matrix transformer [45] (transformer made of several primaries with individual magnetic cores and with only one secondary winding that encloses all the cores) was proposed in 2001 [46] [47]. It can be considered as a topological variation of the monolithic transformer modulator. The pulse transformer is equipped with several primary windings with low number of turns in order to minimize the equivalent leakage inductance, and to obtain shorter rise and fall times. This topology also allows the utilization of standard IGBT technology (<3.3 kV), as the voltage can be adapted with the transformer ratio and the current shared among the different primary circuits. The topology is illustrated in figure 16.
In the last years, this topology has been further studied and optimized for recent applications at ETH Zurich [48], particularly concerning the design of matrix transformers for pulsed applications [49]. This modulator topology is also commercially available from Scandino\textsuperscript{a} and Ampegon\textsuperscript{\textregistered}.

In addition to the shorter rise and fall times, this topology also provides natural current balance among the primaries, as the magnetic flux is common. However special care must be taken to achieve a synchronous switching in all the primary circuits. Unbalances and over-voltages could occur, increasing the risk of damaging the main switches of the slower primary circuits. Despite its modularity, the system cannot continue operating correctly if there is a problem on one of the primary circuits (e.g. broken main switch). No results regarding power fluctuation and power consumption have been published up to date, even though this modulator topology does not naturally operate at constant power consumption.

### 2.1.10 SPRC Modulator

As an evolution of the Polyphase Resonant Converter Modulator and the Thomson Modulator topologies, a new topology consisting in the series connection of DC-DC modules based on resonant topologies was proposed in [50] [51]. The topology was further studied and optimized at ETH Zurich [52][53][54]. Each individual module is composed of a Series Parallel Resonant converter (SPRC) which includes a full bridge, a series parallel circuit, a transformer, a rectifier and a capacitor filter (see figure 16).
Instead of using one single pulse transformer to amplify the voltage, like the Thomson topology, several modules are connected in series in order to achieve the output high voltage ratings, as illustrated on figure 18. The size of each individual isolation transformer is relatively small due to its high frequency operation. Several SPRC modules can be parallelized to achieve higher power ratings and also interleaved, to further reduce the ripple levels. Each module operates with zero voltage switching (ZVS), and efficiency levels of 94.7% have been reported.

The main advantages of this topology are the modularity and the fact that a pulse transformer is not required. On the other hand it exhibits slow rise and fall times due to the fact that the control bandwidth of the individual SPRC modules is limited by their resonant frequency.

### 2.2 Droop Compensators

Although several modulator topologies inherently present voltage droop compensation mechanisms to create an accurate output voltage pulse flat-top [55, 56], the most used modulator topologies require an
additional circuit to compensate for the discharge of the main capacitor bank and also, in the case of transformer-based topologies, for the voltage drop across the transformer internal impedance. This additional circuit is called “a bouncer”. Despite the fact that some droop compensation solutions have been presented in the literature for specific topologies (like for the Marx generator for example [13]), their application could potentially be extended to other klystron modulator topologies. For this reason voltage droop compensation solutions, not necessarily restricted to the monolithic modulator topology, will be presented hereafter.

2.2.1 Passive Bouncer

A simple compensation circuit, proposed by Fermilab and DESY in 1993, consists in the series connection of a resonant LC circuit to the main capacitor bank and the pulse transformer primary winding [40]. By triggering the passive bouncer before the pulse, the quasi-linear part of the longer period sinusoidal voltage oscillation of the LC circuit can be used for voltage droop compensation, as shown in figure 19.
In transformer-based modulators, this LC or passive bouncer circuit is usually connected in series to the transformer primary side, which typically requires the utilization of high current switches. If this circuit is installed on the secondary side, all the bouncer components (HV switch, diode, capacitor and inductance) must sustain high voltage ratings. Other authors have proposed a topological modification of this circuit [57, 58] in order to use it in the secondary side without the need of high current or high voltage switches. This modification is based on the utilization of a specific transformer whose leakage inductance plays the role of the inductance in the passive LC bouncer. This topology, known as the two-winding inductor bouncer circuit, is depicted in figure 20.

Modulators using this compensation scheme achieved 0.5% pulse flatness in short pulse applications and 1% in long pulse ones. Even though this circuit presents some advantages, like the absence of high-frequency ripple and its simplicity, it also presents some drawbacks. For instance, it only uses the quasi-linear part of the
sinusoidal oscillation and becomes bulky for long pulse applications. In addition to this, it operates in open loop, which means that it relies on a pulse to pulse charging voltage correction, and it is very sensitive to pulse length and load changes.

![Diagram of Transformer based modulator equipped with two-winding inductor bouncer](image)

**Figure 20** Transformer based modulator equipped with two-winding inductor bouncer

### 2.2.2 Active Bouncer

As an alternative to the passive bouncer, an active bouncer operating in closed loop was designed and constructed at CERN [59]. This bouncer circuit is composed of a multiphase buck converter with a damped output filter, as depicted in figure 21. In addition, a diode has been placed in parallel to its output filter in order to prevent the modulator current from flowing through the output filter capacitor, violently discharging it.
The connection of this system to a modulator has not been yet performed. However, from numerical simulation results, we can state that the active bouncer achieves better performances and is more efficient than a passive one. The high bandwidth of this system makes possible the closed-loop regulation of the output voltage pulse flat-top and the possible disturbance rejection. It can also be used to potentially reduce the transformer rise time by boosting the primary voltage at the beginning of the pulse.

![Figure 21 CERN LINAC4 Active Bouncer Prototype](image)

**2.2.3 Vernier Cells**

This droop compensation system, used in the P1-Marx Modulator, is based on compensation cells, called Vernier cells [60] [61], which prevent the discharge of the capacitor bank on each main cell, by recharging it during the pulse, using the topology depicted in figure 22.
The achieved pulse flatness using this system was 0.5% and SLAC was able to reduce the energy stored in Marx cells from 1.5 MJ to roughly 100 kJ. The designers claim that, compared to a bouncer-type correction, this scheme can compensate a larger droop up to ~40% with reduced size and cost. However, experiments were performed with an important number of Vernier cells [16], meaning that each cell has limited compensation capability. Despite the modularity of the design, the important number of cells can have an impact on reliability. In order to solve this issue, parallel redundancy should be implemented, with higher cost.
2.2.4 Buck Regulator Cell

A different compensation scheme designed for the Marx-P2 modulator consists in adding a buck regulator to each cell [62] [63]. The regulator keeps the voltage constant in the cell during the pulse. The topology is shown in figure 23.

Using this compensation technique, a pulse flatness of 0.1% was achieved. Compared to the Vernier cell scheme, the system is now completely modular. The cells present the same structure and ratings, and reliability is increased. However the control scheme does not use feedback to adjust the output during the pulse (the regulation is performed by a single computer from pulse to pulse) and, thus, the system is sensitive to disturbances and load changes. Another drawback of this solution is the amount of energy stored due to the addition of another capacitor bank per cell.

Figure 23 Marx cells equipped with buck regulator
2.2.5 Inductance capacitor type filter

Another droop compensation system, also designed for the Marx Modulator, consists in an inductance capacitor filter [64]. This filter is added to one of the Marx cells, which becomes the droop compensating cell in the Marx cascade (see figure 24).

The current in the droop compensating cell filter inductor is ramped to the load current before the pulse, discharging the filter capacitor through the closing of the droop compensating Marx cell main switch. During the pulse, when the current falls below the load reference, the Marx cell switch opens, and the current circulating through the bypass diode loop charges the output capacitor, increasing its voltage and providing voltage droop compensation. The slope of the voltage droop compensation is determined during the design phase, by selecting a correct value of the filter inductor. At the end of the pulse, the energy of this output capacitor is recovered to the filter capacitor using a step-up discharge transformer.

This solution presents some advantages, because it does not require an auxiliary power source or a complex controls system. However it has very little flexibility once the optimal inductance value is calculated during the design phase, and no experimental results have been presented since its publication in 2008.
2.3 Constant power consumption

As explained previously, the important number of modulators has a strong impact on the total power consumption and on the connection of the whole CLIC modulator complex to the grid. The power fluctuation (difference between the peak power consumption and the average power consumption) must be minimized due to the limited peak power available at the connection point, but it also has to be attenuated for other reasons. For instance, power fluctuation can cause voltage flicker. This attenuation can be performed by passive filtering on the AC side, or directly at the modulator level. The obligation to use standard grid components like switchgears requires the utilization of a specific number of transformers at predefined standard voltage levels. The grid layout is then imposed and the distribution transformers fix a given amount of voltage fluctuation versus a given fluctuation in current, as a consequence of power fluctuation. Even though several norms exist regarding the maximum levels of disturbances to the mains (i.e. standards EN 61000, IEC 1000-3-7, ...), these values can actually be negotiated with the grid provider.
An ideal solution to the power fluctuation issue would consist in a modulator system already able to operate at constant power consumption, as the AC passive filtering can have a very important impact on civil engineering due to the capacitors volume [65]. The Thomson modulator is the only modulator able to operate at constant power consumption, but with much lower repetition rates and longer pulses than with the CLIC case. A study about constant power capacitor chargers for the monolithic modulators of the superconducting linear accelerator (TESLA) was carried out by DESY [66, 67] in 2000. The designers identified that the voltage in the modulator capacitor bank only discharges partially. Therefore, the capacitor bank voltage can be split into the sum of a DC part and a varying part. Based on this concept, they identified two possible topologies based on the series connection of two power converters, one providing a DC voltage and a DC value, and the other one providing a varying voltage and current operated under a constant power loop. Both topologies, depicted in figures 25 and 26, are based on a diode rectifier, which provides the constant DC part of the total voltage, associated to a SCR bridge or a switched mode power supply, that is delivering the varying part of the voltage, as shown in figure 27. In this scheme, the diode rectifier operates at constant voltage and constant current, while the SCR bridge or switch mode power supply is regulated to operate also at constant power. The operating principle of these supplies has been proven in simulations, but no experimental results have been published.

![Figure 25](image.png)

*Figure 25 Series connection of a Diode and a SCR bridge for constant power consumption*
2.4 High bandwidth – Low Ripple Power Converters

CLIC klystron modulator specifications require the design of an active droop compensator (active bouncer) with high bandwidth, low ripple and high efficiency, in order to respect the challenging modulator output voltage pulse specifications. One of the challenges in the design of such a converter consists in the dimensioning of the output filter, whose role is to attenuate harmonics produced by the switching frequency ($f_s$). However, the output filter can limit the high bandwidth requirements due to a low cut-off frequency. In addition, when very high performances and high efficiency are required, the maximal tolerable switching frequency is limited by the switching losses and can be in the order of the specified voltage bandwidth, introducing several design challenges.
2.4.1.1 Multiphase buck converters

In order to achieve a minimum closed-loop bandwidth and a given output voltage ripple amplitude, the design of a single-phase buck converter consists on a trade-off between output filter size and switching frequency. A light output filter requires higher switching frequency in order to maintain the same output voltage ripple value, implying higher switching losses and higher magnetic losses in the output filter inductance due to an increase of the peak-to-peak current ripple. This problem becomes more important in high power applications, as higher power switching modules usually present higher switching losses. On the other hand, a bulky output filter relaxes the required switching frequency to achieve the same output voltage level, but it can limit too much the system bandwidth and increase too much the size of the system. A solution to cope with this challenge consists in interleaving several basic topologies such as buck or H-bridges, illustrated in figure 28, and combining them in series or in parallel. Interleaving appears to be a way to improve the transient response, to achieve output ripple cancellation (resulting in reduced total inductor current ripple and output voltage ripple), increase output filter impedance, increase reliability and decrease thermal stress (lower losses per switch and reduced current per phase); however it also presents many challenges in order to get the full benefits of this topology introduces additional problems, that will be discussed hereafter.
2.4.1.2 Topological solutions for high-bandwidth/low-ripple power converters

Different output filter topologies and design strategies for achieving optimal designs of high-performance multiphase power converters are possible. This section reviews different output filter design strategies and topological variants that have been proposed in the literature.

2.4.1.3 Design of high bandwidth output filter for multiphase buck converters

In order to increase the energy transfer speed during transients, and thus the bandwidth of the system, a smaller output filter inductance is desirable. Quasi-square-wave topology (QSW) reduces significantly the inductance, resulting in high peak-to-peak ripple. Interleaved QSW has been proposed in [68] to overcome this...
problem, and even though the efficiency and the bandwidth of the system are improved, the per-phase peak-to-peak ripple remains high, causing an increase in conduction losses. Moreover, its benefits are based on the output current ripple cancellation that, even if it is theoretically possible, a perfect cancellation is difficult to achieve in practice due to delays in the system, differences in the value of the output filter inductances, etc.

As the bandwidth is also determined by the closed-loop control strategy, it has been shown [69] that smaller inductances do not necessarily improve transient response and, thus, it exists a trade-off point. Taking into account the control bandwidth and the desired current step-up dynamics, it is possible to calculate the biggest inductance value that avoids duty cycle saturation during transients. As a consequence, the concept of a “critical inductance” design has appeared as the largest inductance value that gives the fastest transient response. Compared to QSW, it provides the same transient response but with a smaller current ripple.

Parasitic components in the output filter also have negative effects on the bandwidth. A high equivalent series inductance ($ESL$) restricts the speed at which the capacitor can provide current, and a high equivalent series resistance ($ESR$) limits the largest current the capacitor can provide to the load. It has also been shown that parasitic parameters form resonant loops causing transient voltage drop spikes [68, 70], and thus its effects should not be ignored when analyzing the transient response. In order to reduce their impact, several capacitors must be parallelized. Critical inductance design also mitigates this effect. The relation between bandwidth and the transient voltage spike was studied in [59], showing that when the bandwidth is high enough, the $ESR$ of the output capacitor limits the transient voltage spike; however, for low values of control bandwidth, it is the control bandwidth that determines the transient voltage spike. A “critical bandwidth” exists that separates the two zones.

In the pulsed power domain, the system bandwidth can approach the switching frequency, and the design of the output filter becomes more and more critical. Typical un-damped second order $LC$ output filters present a peak at the resonant frequency, as shown in figure 29. As a result, the harmonics at the switching frequency would not only be amplified, but they would also be fed-back by the closed-loop controller. In order to avoid this effect, a damped filter [71] with an additional $RC$ branch (see figure 29) is desirable.
2.4.1.4 Output filter inductances of multiphase buck converters

Inductances generally present a significant tolerance value. The differences in the inductance values results in asymmetry of phases [72], reducing the ripple cancellation and producing additional phase delay. As a consequence, a current ripple at the switching frequency appears at the output making their attenuation difficult, since the filter has been designed for \( m \) times the switching frequency (\( m \) is the number of phases). This effect becomes more important as the number of phases increases. A Monte-Carlo approach has been suggested in [73] for worst case estimation of the output ripple based on inductance tolerance value and number of phases, due to the complexity of modeling an analytical expression.

Although multiphase interleaved topology reduces the current ripple stress in the output capacitors, due to the ripple cancellation feature, it cannot reduce the current ripples on each phase. Coupled inductor structures have been proposed [74, 75] to reduce the steady-state current ripple without compromising the transient response. By coupling the inductances, the converter has large equivalent inductances in steady-state operation and smaller equivalent inductances in transient response. It has been shown that when the coupling coefficient is high enough, it is possible to push the bandwidth from 1/6 to 1/3 of the switching frequency maintaining the same phase margin.
2.4.1.5 Output Filter Topological Variants

The utilization of an additional capacitor bank charged at a higher voltage to store the extra charge required during the step-up transient has been proposed in [76]. The main capacitor bank could also be used to sink the current during the transient by shorting it to ground. By using different RC constants and by taking into account the capacitor ESR, it is possible to design a combined solution where two branches, a fast one and a slow one, provide current during transient. An Active Clamp Circuit connected in parallel to the output of the switching regulator, as shown in figure 30, has also been proposed in [77]. When a transient perturbation exceeds a certain tolerance band, the active clamp circuit connects the load to a pre-charged capacitor bank or sinks the current to a ground reference.

![Multiphase Buck and Active Clamp](image)

**Figure 30 Multiphase buck converter (3-phases) equipped with an active clamp circuit**

Multicell topologies with flying capacitors have also been studied. A comparison between a three-level (two-cell) buck converter and a two level classical multiphase converter shows that the multicell topology achieves the same performance using only one inductor in the power stage at the expense of higher conduction losses [78].
2.4.1.6 Output filter Linear Output Stage

Hybrid sources, as the one shown in figure 31, also called Quasi Linear DC/DC converters, have been studied as a solution to achieve fast transient response and bandwidths beyond the switching frequency [79]. A hybrid design with very low ripple has been studied, where the output bandwidth is imposed by the linear stage [80]. Furthermore, this approach allows the reduction, and even the elimination, of the output filter capacitor. Although no significant reductions of efficiency have been shown in low voltage applications, this approach still needs to be studied in medium voltage IGBT based topologies by evaluating the linear stage power losses during large transients. Nevertheless this solution seems a promising alternative for achieving power converter designs with low switching frequency, high bandwidth and very low ripple.

In order to combine the benefits of linear regulators and capacitor filtering, the hybrid filter concept has also been investigated [81]. This approach considerably relaxes the requirements of the linear stage. The paralleled linear regulator is designed to provide the transient current during the time the passive power filter takes to react to transient perturbations. Its output current is greatly reduced if we compare it with the hybrid source solution, where the linear output current is designed to respond to the maximum transient current step during short periods of time. The hybrid filter concept is especially interesting to reduce output ripple, particularly at the switching frequency, and to achieve an important bandwidth improvement without degrading the system efficiency.

![Figure 31 Multiphase buck with an additional Linear Output Stage](image_url)
2.4.2 Control solutions for multiphase power converters

The control of multiphase power converters introduces additional complexities in comparison with a single-phase power converter application, like sideband harmonics, steady-state limit cycling oscillation or specific control strategies to achieve a correct balancing of the current among the different phases while maintaining the performances of the output voltage control loop. This section reviews these specific phenomena for multiphase power converters, and presents relevant solutions presented in the literature to optimally solve these limitations.

2.4.2.1 PWM Harmonics

It has been shown that the classical average model is not suitable to predict high frequency behavior [82]. Its validity is limited up to 1/6 of the switching frequency for control studies purposes because of the additional phase margin loss introduced by the PWM average pure lag.

PWM also produces additional harmonics. The most important part of these harmonics are situated at the perturbation frequency, $f_p$, and around the switching frequency $f_s$. These harmonics are also called sideband components (see figure 32). A special case occurs when the perturbation frequency is equal to half the switching frequency, due to an aliasing effect between harmonic components (figure 32.b).

The effects of these harmonics are not only visible at the output; as these perturbations are also fed-back by the control voltage feedback loop and reproduced again at the input of the PWM comparator. In order to model analytically the effects of the sideband components and thus predict the high frequency behavior, Sample Data and Harmonic Balance methods have been considered. However their complexity has been also highlighted. In [82] Extended Describing Functions were selected to model the non-linear part in the frequency domain, based on the fact that Harmonic Balance can be considerably simplified for the buck converter. Closed loop analysis shows that the feedback loop operates as a low pass filter that is able to attenuate the sideband components for low values of the perturbation frequency, but as the perturbation frequency increases, the $f_p-f_s$ harmonic decreases its value producing undesirable phase drop. A minimum switching frequency can thus be calculated to guarantee a given performance for a given signal bandwidth.
2.4.2.2 PWM Resolution

The presence of steady-state oscillations at frequencies lower than the switching frequency in PWM controlled converters, particularly in the output voltage, has been evaluated as a result of quantization effects. When the PWM resolution is lower than the ADC resolution it exists a zero-error bin, an actuation value without a specific level in the PWM, as shown in figure 33. Therefore, the PWM controller tries to map it around two PWM levels, resulting in steady-state limit cycling. Conditions for their elimination are suggested in terms of control law, ADC and PWM resolution [83].

As the number of bits of precision and switching frequency is increasing, the design of the PWM comparator presents more difficulties. In order to increase the effective PWM resolution without also increasing the frequency
of the modulation ramps, dithering and sigma-delta modulation have been proposed, however dithering can increase also the output ripple. Different dither patterns and multilevel dithering can improve this issue [83].

Some authors have pointed out the benefits of using double-edge modulation instead of single edge in reducing the phase delay at high frequencies. However, it has been shown in [84] that this reduction is strongly related to the duty cycle. As the type of modulation changes, the output ripple levels versus duty cycle also change.

In order to reduce the effects of phase mismatch and sub-harmonic ripple, the zero-error bin approach has also been utilized. By increasing its value, it is possible to make these effects not visible for the digital control loop. As pointed out in [85], this result could also be achieved through digital filtering. A non-linear gain PWM has also been proposed [86], improving the noise rejection by slowing the response around the steady state operation point.

![Figure 33 PWM zero-error bin](image)

2.4.2.3 Phase Ordering Methods

The difference in the value of the output inductances produces a different current ripple in each phase that compromises the output ripple cancellation. As a result, the output ripple is not only higher, but also a sub-harmonic at the switching frequency appears at the output, making its attenuation more difficult.

A phase ordering method has been proposed [72] to reduce the output current ripple. By modifying the phase switching order, for instance shifting two of the phases with similar ripple by 180° in a 4-phases multiphase buck converter, it is possible to achieve better ripple cancellation, as shown in figure 34. During the power converter first start-up, this method first pulses each phase individually and measures the current rise slope to identify each phase inductance value. With the values of the inductance of each phase, an optimal phase
ordering that minimizes the total current ripple can be calculated. This solution has been demonstrated for a 16-phase converter where phase pre-order arrangement achieved a 50% ripple reduction in [85].

Figure 34 Ripple reduction obtained by modifying the phase order in a 4-phase interleaved buck converter

2.4.2.4 Digital Control Loops Optimization

The design of the control method for multiphase converters needs to guarantee, in addition to an increase in the control bandwidth for a given switching frequency, a correct sharing of the current among the phases. Peak current control greatly simplifies the current balancing; however sample and hold effects cannot be cancelled in multiphase converters [87]. This strategy introduces a pair of double zeroes at half the switching frequency and the voltage loop is not able to compensate such a fast phase decrease. If one also considers the sideband frequency components generated by the PWM comparator, no obvious improvement in terms of bandwidth is achieved by interleaving when comparing with the single phase case [82, 84]. One of the proposed solutions is to introduce external ramps at the input of the PWM comparators in order to reduce the influence of the current loop (resulting in a compromise between peak current control and voltage-mode control) and
separate the double poles of the transfer function. Once separated, the compensation of the single poles is easier and thus the bandwidth can be pushed further.

Voltage-mode control in multiphase converters can theoretically cancel the effects of the sideband components and achieve a bandwidth equal to $m$ times the switching frequency ($m$ being the number of phases) but in reality it is not possible because of the component tolerances. In order to share the current among the phases, a current sharing loop is necessary. With the current sharing loop, since part of other phases current information is utilized in the current loop of one phase, the influence of the switching frequency ripple is reduced at the expense of an increment in magnitude of higher frequency harmonics (integer multiples of $f_s$).

$V^2$ control [88, 89, 90] has also been proposed to improve the transient response. It is composed of two voltage control loops, a slow one to regulate the output voltage without steady-state error and a fast reaction loop fast that is directly added to the input of the PWM comparator, and one current sharing loop. Although $V^2$ control is able to achieve a very fast load step-down transient, the load step-up is limited by the switching action delays in the PWM. On the other hand, constant on-time control, with a similar control structure, achieves a very fast load step-up, however the constant on-time limits the load step-down.

In order to further achieve a very fast transient response, hybrid control methods have also been studied [91, 92, 93, 94], in particular containing non-linear controllers in order to reach ideal transient responses. In linear-nonlinear control, a combination of a hysteresis controller and a linear controller working inside the hysteresis band has shown very good performances, though special care should be taken during the design to avoid chattering. A combination of a linear controller and a bank of switching surface controllers has also been presented [95], obtaining fast large signal transient responses and precise control in steady state.

### 2.5 Conclusion

This chapter presented the state of the art of klystron modulators, voltage droop compensators and high bandwidth and high performance power converters. None of the existing klystron modulators presented in the literature is capable of achieving the CLIC drive-beam klystron modulator in terms of output voltage pulse quality and constant power consumption from the grid. As a conclusion, new topological solutions able to achieve these critical requirements for CLIC must be found. From previous results presented in the literature, droop and voltage compensators for CLIC must be active, due to the high bandwidth and low ripple design required to respect the output voltage pulse specifications during the 140µs pulse. Purely passive solutions would introduce an unacceptable size and cost increase.
Multiphase interleaved buck converters seem to be the best topological candidate to achieve the high bandwidth and low-ripple design required for the CLIC active bouncer, and will be taken into account in the next chapter, where topological solutions able to perform the voltage droop and power compensation tasks will be investigated. The presented output filter topological variants and different control solutions for multiphase power converters will be evaluated and explored in the next chapter, in order to select a final topology for the CLIC klystron modulator.
CHAPTER III

3 CONVERTER TOPOLOGY RESEARCH

The previous chapter presented a detailed state of the art of klystron modulators, droop and power compensators, which concluded that state-of-the-art solutions do not fulfill CLIC specifications. Following the R&D strategy established by CERN introduced in chapter 1, this research work focuses on the monolithic transformer based modulator topology. In this chapter, two new topologies for modulators based on a monolithic pulse transformer able to respect CLIC requirements are proposed and studied in detail.

A classical monolithic transformer based modulator topology is composed of a high voltage DC capacitor charger, a main capacitor bank, a bouncer circuit, a step-up transformer and a single high voltage switch, as shown in Figure 35. The main capacitor bank can be controlled using several control strategies, which present very important differences in terms of power fluctuation. For the sake of simplicity, if we consider the equivalent circuit of figure 36, the capacitor charger can be operated in three different ways. Figure 36.A) shows a typical practice in pulsed applications, consisting in disabling the charging action during the pulse in order to protect the capacitor charger against overcurrent. With this mode of operation, a charging power fluctuation of 100% is obtained. If the capacitor charger converter is a direct topology (i.e. without internal storage elements), the charging power fluctuation corresponds to the AC power (P_{AC}) fluctuation (the instantaneous active AC power equals the instantaneous charging DC power V_{CH} I_{CH}). In order to attenuate the power fluctuation, the charger can also be operated at constant charging current as illustrated in figure 36.B). This operating mode is able to reduce the power fluctuation; however, the not controllable voltage fluctuation across the capacitor C_{main} (V_{CH}) still presents variations, which are translated in power fluctuations. A third and final case is presented in Figure 36.C), where the charging current is controlled in order to maintain the charging power constant, as shown in equation 5.

\[ I_{CHref} = \frac{P_{average}}{V_p} \]  

Although this is a viable solution, a very high current bandwidth from the capacitor charger is required for fast pulsed systems. This issue becomes a real limitation in high voltage applications, as high voltage capacitor chargers present a finite, and usually low, current bandwidth.
Figure 35 Classical monolithic modulator topology

Figure 36 Capacitor charger control strategies
3.1 Dual Purpose Active Bouncer DPAB

One option to cope with this problem would consist in trying to drastically increase the bandwidth of the capacitor charger. However, due to the high voltage output ratings, this is quite difficult. As an alternative solution, a new topology shown in figure 37, which utilizes an active bouncer connected in series with the main capacitor bank, forming a parallel branch to the high voltage capacitor charger, is proposed. This topological modification makes possible to use the active bouncer not only to compensate the capacitor and transformer voltage drop during the pulse as in a classical topology, but also to regulate the primary voltage from pulse to pulse in order to maintain it constant. This solution also simplifies the requirements of the high voltage capacitor charger, making possible to use a standard commercially available power supply, as now it can operate simultaneously at constant voltage and constant current.

The topology is named Dual Purpose Active Bouncer (DPAB) [97], as it combines the tasks of both droop and power compensation into a single power converter.

The active bouncer is designed in such a way that is able to compensate up to a certain percentage of voltage droop, depending on the primary voltage ratings and the selected active bouncer switch technology. With the purpose of optimizing its performance, a four quadrant operation is required in order to recharge its own capacitor bank from the modulator high voltage capacitor charger current, eliminating the need for an additional capacitor charger for the active bouncer, and also to double the operating voltage range from the switch technology ratings. The modulator main capacitor bank is dimensioned according to the active bouncer maximum output voltage ratings. With such an approach, defining \( V_{b_{\text{max}}} \) as the maximum voltage the DPAB can provide at its output, it experiences during the pulse a maximum discharge of 2\( \times V_{b_{\text{max}}} \) (please notice that the

![Figure 37 DPAB topology](image-url)
reason to specify in this way the active bouncer output range is because of its bipolar voltage capabilities). Figure 38 shows the waveforms of the voltage, current and instantaneous power in the active bouncer during a 20 ms cycle (50 Hz repetition rate).

The operation of the system can be divided in two phases: pulsing and charging. At the beginning of the pulsing phase, the main capacitor bank of the modulator is charged at a voltage equal to \( V_{kn} + V_{b_{max}} \), being \( V_{kn} \) the average main capacitor bank voltage and \( V_{b_{max}} \) the maximum voltage droop compensated by the DPAB. When the main switches closes, the main capacitor bank starts decreasing its voltage to \( V_{kn} - V_{b_{max}} \). During this time, the active bouncer output voltage increases from \(-V_{b_{max}}\) to \(+V_{b_{max}}\), in order to compensate the discharge of the main capacitor bank. Just after the pulse, the main switch opens and the current drops down to \( I_{ch} \) until the next pulse. During this time the output voltage of the bouncer decreases slowly back to \(-V_{b_{max}}\), in order to maintain the primary voltage constant, as the main capacitor bank recharges.

It is important to notice that the active bouncer capacitor bank is recharging and discharging not only during half of the charging phase, but also during half of the pulsing one, as depicted in the instantaneous power graph shown in figure 38. Therefore, by offsetting the output voltage operation of the DPAB, it is possible to achieve a zero energy flow during one complete 20ms cycle, due to the fact that ideally the DPAB provides and recovers the same amount of energy.
3.1.2 DPAB Design

3.1.2.1 DPAB Output Filter

The design of the active bouncer output filter presents some challenges. At first glance it could seem that a typical LC filter with a high cutting frequency could be used, as the active bouncer only compensates a small percentage of the primary voltage and its switching harmonics would only be a fraction of it. However one has to notice that, at the moment of the closing of the main switch, a current equal to $I_{kn} = \frac{1}{R_L}$ will suddenly flow into the active bouncer filter capacitor, discharging it. A simplified modulator circuit is shown on figure 39 to illustrate this phenomena: when the main switch of the modulator closes, the primary current $I_P$ rises very fast to its nominal value, while the active bouncer is not able to compensate this current perturbation until the current on its output filter inductances $I_B$ does not rise up to the same primary current nominal value. The current flowing
through the active bouncer filter output filter capacitor being \( I_B-I_P \), a very important current large signal bandwidth is then required to minimize this transient.

Figure 39 Pulse current perturbation

As shown on figure 40, an ideal active bouncer consists of an ideal voltage source, meaning that it would be able to impose any voltage at its output independently of the current flowing through it. However, due to the fast current step to high current values in the \( kA \) range and also due to the fact that a real power converter has an internal impedance (figure 40.C), the current flowing through it has a direct effect on the output voltage. Therefore it can be modelled as an external perturbation that needs to be compensated.

A multiphase approach could help to increase the current bandwidth. However, an infinite current bandwidth would be ideally required to perfectly compensate the current perturbation. Consequently, an increase of the output filter capacitor value in order to reduce the voltage discharge excursion during the first moments of the pulse is also required.
Another aspect to take into account when designing the active bouncer output filter is the variation of its voltage transfer function in the two modes of operation corresponding to the pulsing and charging phases. The harmonics attenuation is much higher during the pulse, as the load has capacitive characteristics. However, during the charging phase, as the transfer function between primary voltage and active bouncer output voltage is 1, special care must be taken in order to damp the active bouncer voltage transfer function. In order to design a filter that is suitable for the two different phases, a resistively damped LC-4C filter is recommended.

3.1.2.2 Capacitor bank size

When dimensioning the size of the active bouncer capacitor bank it is important to notice that the special power cycles previously depicted on figure 38 must be taken into account. As the active bouncer is ideally absorbing and delivering the same amount of energy during the pulsing phase, if there is enough voltage at the beginning of the pulse in the bouncer capacitor bank, no further charging requirements would be necessary. However, during the long charging phase the active bouncer is first providing and afterwards absorbing energy. Hence, the capacitor size must be high enough in order to guarantee that there is always enough DC voltage in the active bouncer capacitor bank to continue operating correctly. As an example, if the designers decides to allow a voltage discharge of 20% of the active bouncer capacitor bank, in order to have still enough input voltage to react, the capacitor value must be calculated as shown in equations 6 and 7.

\[
\frac{1}{2} C_{\text{bouncer}} V_{\text{bmax}}^2 - \frac{1}{2} C_{\text{bouncer}} (0.8 \times V_{\text{bmax}})^2 = I_{\text{CH}} \cdot \frac{V_{\text{bmax}}}{2} \cdot \left( \frac{L_{\text{RE}} \times f_{\text{flat}}}{2} \right)
\]

5 Energy analysis considers the fact that energy is only recovered during half of the charging cycle, when \(I_{\text{CH}}\) is negative and \(V_b\) positive.
\[ C_{\text{bouncer}} = \frac{I_{\text{ch}} V_{\text{bmax}}}{V_{\text{bmax}}^2 - (0.8v V_{\text{bmax}})^2} \]  

(7)

One must notice that no losses in the active bouncer have been considered in this first simplified energy analysis. In the real model, in order to fully recharge the active bouncer capacitor bank after every cycle, a small DC supply would be required to compensate the losses in damping resistor of the filter, switches operation, etc.

### 3.1.2.3 DPAB Power Converter Topology

In order to achieve a 4-quadrant operation and achieve a large signal current bandwidth, a multiphase interleaved H-bridge topology is proposed, as illustrated on figure 41. On one hand, the required number of phases will be a function of the large signal current bandwidth required to compensate for the initial current perturbation and avoid the discharge of the active bouncer output filter capacitor. On the other hand, the number of phases will also depend on the maximum switching frequency IGBT that can be achieve on each H-bridge leg, in order to achieve the required closed-loop voltage bandwidth in the active bouncer.
3.1.2.4 DPAB Control Strategy

There is a drastic difference between the two voltage transfer functions for each DPAB operation phases. During the pulsing phase, the modulator capacitor bank and the load, provide additional harmonics damping (transfer function between $V_{in}$ and active bouncer output voltage). However, during the charging phase, as the transfer function between $V_i$ and active bouncer output voltage is 1, the DPAB output filter is the only element providing damping to the switching harmonics. To solve this issue, a control strategy using a different voltage control loop specifically optimized for each converter phase is proposed. The selected controllers consist in two RST digital controllers [96] that are able to compensate the dynamics and handle the important and different

![Figure 41 DPAB converter made of multiphase interleaved H-bridges](image)
delays of the system. Due to the multiphase interleaving solution proposed for the active bouncer topology, an additional low gain current sharing loop, able to balance the current among the different phases, has also been considered. Figure 42 illustrates the proposed control strategy.

![Control Strategy Diagram](image)

**Figure 42 DPAB Control Strategy**

### 3.1.3 DPAB Simulation and Performance Evaluation

With the purpose of validating the correct operation and evaluate the performances of the proposed Dual Purpose Active Bouncer system, a simulation considering CLIC specifications has been carried out. For a primary voltage of 15 kV, a modulator main capacitor bank of 150 µF has been selected in order to produce a discharge of 1600 V during the pulse. The transformer equivalent circuit parameters referred to the primary side, and the active bouncer specifications imposed, are presented in table 2. Figure 43 shows the simplified schematic of the modulator equipped with a DPAB considered in the simulation.
Table 2 DPAB, pulse transformer and klystron equivalent circuit simulation parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Active Bouncer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equivalent Capacitance: 86.7 nF</td>
<td>DC bus: 1000 V</td>
</tr>
<tr>
<td>Leakage inductance: 3 µH</td>
<td>Inductance value: 25 µH</td>
</tr>
<tr>
<td>Windings resistance: 14.8 µΩ</td>
<td>Filter capacitor: 20 µF</td>
</tr>
<tr>
<td>Magnetizing inductance: 60 mH</td>
<td>Damping resistance: 560 µΩ</td>
</tr>
<tr>
<td>Transformation ratio: 10</td>
<td>Capacitor bank: 2 mF</td>
</tr>
<tr>
<td>Klystron resistance: 9.375 Ω</td>
<td>Number of phases: 5</td>
</tr>
</tbody>
</table>

Figure 43 DPAB simplified simulation model

The results, illustrated on figure 44, show a maximum power fluctuation value of 2.19%. This maximum value is achieved during the pulse step-up settling time, meaning that during the pulsing phase the power compensation is impacted by the output pulse regulation of this phase, due to the pulse step-up settling time and voltage droop across the windings of the step-up transformer.
3.2 Split Power and Droop Compensator SPDC

A second topology is proposed to cope with the challenge of stabilizing the active power at the DC side (product of $I_{CH}$ and $V_{CH}$), with the purpose of achieving constant power consumption. In [65] an analysis of the compromises required to the capacitor charger shows that a high bandwidth control would be required. This might be very difficult to achieve in high power converters (as a reminder the latest developments on CLIC RF power distribution show the need for concentrating the capacitor chargers feeding hundreds of klystron modulators [115]). This new topology splits the output voltage and the charging voltage compensation tasks into two different power converters with independent operation: an Active Bouncer and a Fast Voltage Corrector (FVC), respectively. This new topology, named Split Power and Droop Compensator (SPDC), is illustrated on figure 45.
The two different power converters, FVC and Active Bouncer, are presented hereafter.

### 3.2.1 Fast Voltage Compensator FVC

The FVC power converter is connected in series with the main capacitor bank $C_{\text{main}}$, as a parallel branch to the capacitor charger. The FVC modifies its output voltage to compensate for the charge and discharge of $C_{\text{main}}$, in order to maintain the charging voltage $V_{\text{CH}}$ constant. Figure 46 shows the ideal waveforms of this power converter during a complete modulator cycle.
Figure 46 Ideal FVC waveforms
3.2.2 FVC Design

3.2.2.1 FVC Output Filter Design

For a given pulsed power application, the required charging current in order to charge back the main capacitor bank to its nominal value from pulse to pulse can be calculated as shown in equation 7.

\[ I_{CH} = I_P \cdot t_{flat} \cdot RR \]  \hspace{1cm} (7)

The main capacitor bank is dimensioned in order to experience a maximum voltage discharge, \( \Delta V \), during the pulse, as shown in equation 8.

\[ C_{main} = \frac{t_{flat} \cdot (I_P - I_{CH})}{\Delta V} \]  \hspace{1cm} (8)

A simplified equivalent circuit of the modulator, with the different currents and voltages definitions, is presented on figure 447.

![Simplified equivalent circuit of the modulator equipped with a FVC](image)

Figure 47 Simplified equivalent circuit of the modulator equipped with a FVC

The capacitor charger would ideally consist of a constant current source. The FVC would operate as a voltage source that regulates the charging voltage, \( V_{CH} \). In order to simplify the analysis, a simple \( LC \) output filter has been selected for the FVC. With the purpose of achieving a constant charging voltage, the FVC output filter voltage waveform should follow the same slope as the \( C_{main} \) voltage waveform, but with an opposite sign (see
EQUATING THESE SLOPES DURING THE PULSING AND CHARGING PHASES, THE CURRENT FLOWING THROUGH THE FVC FILTER INDUCTANCE ON EACH PHASE CAN BE CALCULATED, AS IN EQUATIONS 9 AND 10, RESPECTIVELY

\[ I_{FVC\_pulsing} = I_p \cdot \frac{C_{FVC}}{C_{main}} - I_{CH} \cdot (1 + \frac{C_{FVC}}{C_{main}}) \]  

\[ I_{FVC\_charging} = -I_{CH} \cdot (1 + \frac{C_{FVC}}{C_{main}}) \]

WE CAN SEE FROM THESE EXPRESSIONS THAT THE FVC CURRENT ON EACH PHASE IS INFLUENCED BY THE SIZE OF THE MAIN CAPACITOR BANK AND THE FVC OUTPUT CAPACITANCE. FIGURE 48 SHOWS THE IMPACT OF DIFFERENT FVC OUTPUT FILTER CAPACITANCE VALUES ON THE FVC CURRENT, CONSIDERING A MODULATOR RESPECTING CLIC SPECIFICATIONS.

**Figure 48 FVC currents in the pulsing and charging phase for different FVC output filter capacitor values**

ON ONE HAND, WE CAN SEE FROM THE FIGURE THAT, DURING THE CHARGING PHASE, THE FVC CURRENT IS ALWAYS NEGATIVE AND THAT IT PRESENTS A VERY LOW VARIATION WHEN THE FVC FILTER CAPACITOR VALUES ARE INCREASED. ON THE OTHER HAND, THE CURRENT DURING THE PULSING PHASE VARIATES FROM A NEGATIVE VALUE (FOR SMALL FVC OUTPUT FILTER...
capacitance values) to positive value. This implies that the converter would need to be unidirectional or bidirectional in current, respectively. Between the two regions, there is a specific capacitance value for which no current from the FVC would be required during the pulse.

Although the current during the pulsing phase has a little influence on the FVC average current ($T_p << 1/RR$), it has a great impact on the converter topology selection. Therefore, in order reduce the FVC dimensioning power and losses, the general tendency would consist on selecting a low output filter capacitance value. The power flow is another factor that could have an important impact on converter topology selection. If during a complete cycle the FVC supplies and recovers the same amount of energy, a dedicated capacitor charger for the FVC would not be required and, thus, no additional power fluctuation would be generated. Three possible converter topologies are possible: a converter unidirectional in voltage and bidirectional in current (2-quadrant), a converter bidirectional in voltage and unidirectional in current (2-quadrant), and converter bidirectional in voltage and in current (4-quadrant). The first one would require a very high FVC current during the pulse in order to achieve zero average energy, as the pulse time is very short in comparison with the charging time. The remaining two solutions are both interesting; however the bidirectional characteristics in current and voltage allows the utilization of a bigger capacitor bank value, which is the preferred strategy to damp the switching harmonics and achieve a low output voltage ripple. Ideal waveforms of this 4-quadrant topology are shown in figure 49.
In order to complete the output filter dimensioning, a given bandwidth and switching frequency attenuation must be specified. To identify the FVC voltage bandwidth required to respect a given amount of power fluctuation, simulation-based sweeps on a specific modulator model for different FVC closed-loop bandwidths can be performed. As an example, figure 50 shows the results of simulation sweeps for different closed-loop bandwidths performed considering the CLIC modulator specifications.
In this specific example, a minimum closed-loop voltage bandwidth of 15 kHz is required in order to achieve a 1% power fluctuation. By taking a typical design margin of 20% between the closed and the open loop bandwidths, the LC filter can be calculated. The switching frequency can be computed from the voltage output ripple specifications.

3.2.2.2 FVC Control strategy

The FVC load changes during the two operating phases: pulsing and charging. During the pulsing phase the klystron and the main capacitor bank are connected in parallel to the FVC output filter capacitance, providing additional damping to the filter. However, during the charging phase, only the main capacitor bank is connected in parallel to the FVC output filter. In this last case special care must be taken in order to avoid possible harmonic amplifications due to the resonance peak of the LC filter. In order to adapt the FVC regulation to each load case, a dedicated structure made of two different controllers is proposed, as shown in figure 51.
Each controller acts during a given operating phase only. They consist of polynomial RST digital controllers [96], able to specify different dynamics for regulation and tracking. This property is particularly important during the transition between the two operating phases.

3.2.3 FVC Simulation and performance evaluation

In order to validate the performances of the FVC, a numerical simulation considering a modulator respecting the CLIC specifications with a primary voltage of 15 kV, was performed. A single H-bridge topology with a DC bus of 1000 V, a simple LC output filter (100 µH and 7 µF, respectively), and a switching frequency of 100 kHz are considered. Figure 52 illustrates the simulation model, and figure 53 shows the simulation results. Due to the fact that only the power compensation task performed by the FVC is evaluated, the active bouncer has not been considered this example.
Figure 52 FVC simulation model

Figure 53 FVC simulation results
One can notice that the power fluctuation is successfully reduced to a maximum peak of 0.08%. The current in the FVC is positive during the pulsing phase (with a maximum value of 53 A) and negative during the pulsing phase (with a maximum value of -43 A).

3.2.4 Active Bouncer

The task of the Active Bouncer power converter is to compensate the voltage drop due to the main capacitor bank $C_{\text{main}}$ discharge, as well as the voltage drop across the pulse transformer impedance. If we assume that the klystron tube behaves as a resistive load, the modulator current waveform follows the output voltage pulse profile.

A common practice in klystron modulators consists in placing the active bouncer in series with the main capacitor bank $C_{\text{main}}$ and the primary of the pulse transformer [59], as shown in figure 45. However, this configuration presents an issue in applications where the rise time of the pulse is short because, as soon as the main switch closes, all the modulator primary current will suddenly flow into the bouncer output filter capacitor, and discharge it [97]. The active bouncer is not able to compensate this modulator current perturbation until the current in its output filter inductances rises to the same current value, as illustrated in figure 54.A). This perturbation must be taken into account during the dimensioning process of the active bouncer output filter. In [59], an active bouncer circuit with a diode connected in parallel to the output filter capacitor, as illustrated in figure 54.B), was proposed to prevent its discharge to negative values. However, in this configuration the active bouncer is still not able to charge the output filter capacitor to positive voltage values until its output current exceeds the modulator current. Therefore, this configuration is only suitable as a protection for long rise time modulator pulses. A different solution able to initialize the active bouncer output current and speed up the start of the droop compensation action in short rise time applications, like in the CLIC klystron modulator, has to be addressed.
In order to avoid the effects of the modulator current perturbation as previously introduced, a new topology scheme, shown in figure 55, is proposed.

Figure 54 Simplified waveforms of typical active bouncer topologies: A) Multiphase buck converter; B) Multiphase buck converter with blocking diode in parallel with the output filter capacitor.

Figure 55 Proposed Active Bouncer topology
The different operation phases of this new topology are illustrated in figure 56 and described hereafter:

1. **Current initialization**: The short-circuit switch $S_{SC}$ is closed and the active bouncer topology provides $V_{AB}$. As a consequence, the current on the bouncer output filter inductances $I_L$ rises.

2. **Pulse step-up**: The main modulator switch $S_1$ closes. $V_{bouncer}$ rises and $I_L$ continues to increase.

3. **Flat-top**: Once $V_{bouncer}$ achieves its nominal value, the short-circuit switch $S_{SC}$ is opened. The active bouncer topology is controlled to produce an output voltage ramp on $V_{bouncer}$, in order to compensate the $C_{main}$ discharge and to achieve a perfect flat-top voltage $V_{bouncer}$ across the klystron.

4. **Recovery**: The main modulator switch $S_1$ is opened. The pulse transformer is demagnetized through the branch composed by $R_d$, $C_d$ and $D_1$. $V_{bouncer}$ increases its value until it equals $V_{AB}$ voltage. Once this happens, the diode $D_i$ is forward-biased, so the energy stored in $L_i$ is recovered back to $C_{AB}$ passing through the diode $D_i$ and the free-wheeling diode(s) of the active bouncer topology.

5. **Reset**: When the current in the output filter inductances $I_L$ drops down to 0 A, $C_0$ is discharged through a reset resistor $R_R$ by closing the reset switch $S_R$.

Since the short-circuit switch $S_{SC}$ remains permanently closed during the pulse-step up, in order to achieve the nominal current value after the rise time, the current $I_L$ at the beginning of phase 2 must be (the voltage drop across the switch is neglected):

$$I_L(0) = I_p - t_{rise} \frac{V_{AB}}{L_B}$$

where $I_p$ is the nominal primary current of the modulator. Therefore, the initialization of the current must be triggered at the time calculated in (12) before closing the main switch $S_1$.

$$t_{trig\_init} = \frac{L_i}{V_{AB}} I_p - t_{rise}$$

(12)
3.2.5 Active Bouncer Power Converter Topologies

Three power converter topologies, illustrated in Figure 57, are proposed as candidates for the active bouncer. The first one (Figure 57.A) is based on a common multiphase buck-converter topology, as the one presented in [59]. The second and the third consist of a combination of different power converters. They both share a common high-current and low switching-frequency stage (HCS – high current stage), which manages all the modulator current. In addition, a second low-current high-bandwidth stage is connected in parallel. It is used to produce a voltage ramp on the bouncer output filter capacitance to compensate the discharge of the main capacitor $C_{\text{main}}$. In the topology of Figure 57.B, this low-current stage consists of a high switching-frequency buck converter. In the topology of figure 57.C, the low current-stage consists of a power MOSFET operated in its linear region (LS – linear stage).
3.2.6 Active Bouncer Simulation and performance comparative analysis

In order to evaluate their performances, the three topologies have been studied and optimized to respect the CLIC specifications, with the imposed modulator parameters presented in Table 3.

<table>
<thead>
<tr>
<th>Table 3 Fixed modulator parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Modulator Parameter</strong></td>
</tr>
<tr>
<td>Primary Voltage</td>
</tr>
<tr>
<td>Main capacitor bank size</td>
</tr>
<tr>
<td>Klystron equivalent resistance (referred to the primary)</td>
</tr>
<tr>
<td><strong>Transformer Parameters</strong></td>
</tr>
<tr>
<td>Primary winding leakage inductance</td>
</tr>
<tr>
<td>Primary winding equivalent resistance</td>
</tr>
<tr>
<td>Secondary winding leakage inductance</td>
</tr>
<tr>
<td>Secondary winding equivalent resistance</td>
</tr>
<tr>
<td>Magnetizing Inductance</td>
</tr>
</tbody>
</table>
Hysteresis control is selected for controlling the switching stages, while a PI controller is used for the linear stage. The dimensioning procedure is based on a non-linear constrained optimization approach where all the active bouncer component values (including the number of phases) and the controller parameters are considered as optimization variables. The problem constraints are the CLIC modulator specifications presented in Table 1; and the objective function to be minimized is the total active bouncer losses during a complete cycle. In order to reduce the computation time, simplified thermal (switching and conduction losses were evaluated for different 1700V IGBT models) and specific control design models based on bandwidth, gain and phase margins, were used. Results were subsequently validated via numerical simulation. Table 4 presents the calculated active bouncer optimal parameter values for the different topologies respecting CLIC specifications.

Table 4 Optimal Parameters for the three active bouncer topology candidates

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Topology #1</th>
<th>Topology #2</th>
<th>Topology #3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of phases</td>
<td>4</td>
<td>3 x High Current Stage (HCS)</td>
<td>3 x High Current Stage (HCS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 x Low Current Stage</td>
<td>1 x Linear Stage (LS)</td>
</tr>
<tr>
<td>Switching frequency per phase</td>
<td>62.5 kHz</td>
<td>26.3 kHz High Current Stage (HCS)</td>
<td>26.3 kHz High Current Stage (HCS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110.5 kHz Low Current Stage</td>
<td></td>
</tr>
<tr>
<td>Inductance value per phase</td>
<td>100 µH</td>
<td>1.8 mH High Current Stage (HCS)</td>
<td>1.8 mH High Current Stage (HCS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200 µH Low Current Stage</td>
<td>1 µH Linear Stage (LS)</td>
</tr>
<tr>
<td>Output filter capacitance, $C_b$</td>
<td>1 µF</td>
<td>1 µF</td>
<td>1 µF</td>
</tr>
<tr>
<td>Output filter damping branch, $R_{bd}$</td>
<td>0.5 Ω</td>
<td>0.3 Ω</td>
<td>Not required</td>
</tr>
<tr>
<td>Output filter damping branch, $C_{bd}$</td>
<td>4 µF</td>
<td>4 µF</td>
<td>Not required</td>
</tr>
</tbody>
</table>

Figures 58, 59 and 60 show a zoom on the output voltage pulse of 140 µs obtained by numerical simulation for topologies #1, #2 and #3, respectively.

The optimized topology #1 consists of a 4 phases buck converter using 1700V, 800A, IGBTs FZ800R17KF6C_B2 from Infineon. The maximum current and switching frequency per phase are 497A and 62.5 kHz, respectively. It is necessary to damp the LC output filter with a typical $C_b$-$R_{bd}$ parallel damping branch of $C_b=4$ µF and $R_{bd}=0.5$ Ω to avoid subharmonic oscillations. The performances achieved at the secondary output are a voltage stability of 67 V and an equivalent frequency ripple of 250 kHz.
Figure 58 Topology #1 numerical simulation results with optimal parameters based on CLIC specifications.

The optimized topology #2 high-current stage (HCS) is composed of a 3 phases buck converter using the same 1700 V, 800 A, FZ800R17KF6C_B2 IGBTs from Infineon with a maximum current and switching frequency per phase of 644.3 A and 26.3 kHz. The low-current stage is composed of a 4 phases low-current converter using 1700 V, 60 A, BSM50GS120DN2 from Infineon, with a maximum current and switching frequency per phase of 19 A and 110 kHz, respectively. A passive $C_{bd}$-$R_{bd}$ damping branch is still required, with values of $C_{bd}=4 \mu F$ and $R_{bd}=0.3 \Omega$. The performances achieved at the secondary output voltage pulse are a flat-top voltage stability of 49.39 V, and an equivalent frequency ripple of 442 kHz.
The optimized topology #3 high-current stage (HCS) is composed of a 3 phases buck converter using the same 1700V, 800A, FZ800R17KF6C_B2 IGBTs with a maximum current and switching frequency per phase of 644.3 A and 26.3 kHz. The linear stage (LS) is composed of a linear MOSFET based stage with a closed-loop bandwidth of 1 MHz and a maximum output current of 60 A. The damping is performed by the linear stage, so no additional $C_{dc}$-$R_{ds}$ passive damping branch is required in this case. The performances achieved at the output voltage pulse are a flat-top voltage stability of 44 V, and an equivalent frequency ripple of 71 kHz.
The characteristics and performances achieved by the different topologies evaluated by simulation are summarized in Table 5. We can observe how Topologies #2 and #3 increase the filter inductance value of the high-current stage to reduce the switching frequency and, therefore, minimize the switching losses present in Topology #1. The drawback of an increased inductor value is the corresponding increase of the inductor volume, which is proportional to the energy stored ($\frac{1}{2}LI^2$). Topology #3 is the one providing the best performances, due to the high bandwidth of the linear converter. In terms of losses, topologies #2 and #3 are almost two times more efficient than topology #1. Between these two, although the average losses during the pulse are higher on Topology #3 due to the operation of the power MOSFET in its linear region, the lower losses on the bouncer reset (output filter capacitor discharge between pulses) due to the absence of the damping branch (composed of $C_{bd}$ and $R_{bd}$), make topology #3 also the most efficient. In addition, the lower equivalent frequency harmonic content at the output voltage flat-top, simplifies the compensation of its impact on the RF output power, by means of a feedback loop on the low level RF control [98], in order to respect the challenging CLIC repeatability specifications (see Table 1). Therefore, topology #3 seems to be the most convenient one for the future CLIC klystron modulator SPDC active bouncer.
### Table 5 Active Bouncer topologies comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Topology #1</th>
<th>Topology #2</th>
<th>Topology #3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nº of phases High Current Stage</td>
<td>4</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Nº of phases Low Current Stage</td>
<td>-</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>Average losses during the pulse</td>
<td>985 W</td>
<td>446 W</td>
<td>490 W</td>
</tr>
<tr>
<td>Average losses on current rise</td>
<td>7.3 W</td>
<td>43.6 W</td>
<td>43.6 W</td>
</tr>
<tr>
<td>Average losses on current fall</td>
<td>13 W</td>
<td>70 W</td>
<td>70 W</td>
</tr>
<tr>
<td>Average losses on bouncer reset</td>
<td>110 W</td>
<td>110 W</td>
<td>30 W</td>
</tr>
<tr>
<td>Total average losses</td>
<td>1.12 kW</td>
<td>670 W</td>
<td>633 W</td>
</tr>
<tr>
<td>Energy recovered through diode Dc</td>
<td>0.20 J</td>
<td>55 J</td>
<td>55.5 J</td>
</tr>
<tr>
<td>Passive damping required</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Output ripple frequency</td>
<td>250 kHz</td>
<td>442 kHz</td>
<td>71 kHz</td>
</tr>
<tr>
<td>Total magnetic energy stored, LF/2</td>
<td>193.45 J</td>
<td>1.12 kJ</td>
<td>1.2 kJ</td>
</tr>
<tr>
<td>Capacitor bank size</td>
<td>54 mF (1 kV)</td>
<td>60 mF (1 kV)</td>
<td>60 mF (1 kV)</td>
</tr>
<tr>
<td>Output stability at 180kV</td>
<td>67 V</td>
<td>50 V</td>
<td>44 V</td>
</tr>
<tr>
<td>Redundancy modules required</td>
<td>1 module</td>
<td>2 modules</td>
<td>2 modules</td>
</tr>
<tr>
<td>Control &amp; Electronics complexity</td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Main challenges/difficulties</td>
<td>Control Loop</td>
<td>Control + HF stage</td>
<td>MOSFET stage</td>
</tr>
</tbody>
</table>

#### 3.3 DPAB and SPDC comparative analysis

In order to compare the two different CLIC klystron modulator candidate topologies, DPAB and SPDC, the first step consists in comparing the total losses of each solution for a modulator respecting the CLIC specifications. For this first analysis, a voltage droop compensation range of 1 kV, a DC bus of 1.2 kV for the compensators, and a primary voltage of 10 kV is imposed for both topologies.

DPAB topology consists of a 4-quadrant H-bridge topology. For the SPDC, the FVC consists of a 4-quadrant H-bridge topology, and the Active Bouncer is based on the previously presented topology #3. An Infineon FZ2400R17HP4_B9, 1700 V, 2400 A IGBT module equipped with antiparallel diodes and a total $R_C$ of $1 \Omega$, is used for the DPAB single H-bridge, and also for the SPDC active bouncer topology. In the FVC, an IGBT module BSM-200-GB-170-DLC, 1700 V, 200 A, from Infineon with a gate resistance of 10 $\Omega$ is used. The power losses parameters extracted from datasheets are shown in tables 6 and 7, respectively. The same switching frequency value of 20 kHz is considered for all scenarios except for the charging phase of the DPAB topology, where a switching frequency of 5 kHz is selected.
Table 6 Infineon IGBT module FZ2400R17HP4_B9 parameters

<table>
<thead>
<tr>
<th>IGBT</th>
<th>DIODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction</td>
<td></td>
</tr>
<tr>
<td>$V_{CE,0}$</td>
<td>0.75V</td>
</tr>
<tr>
<td>$R_t$</td>
<td>0.646 mΩ</td>
</tr>
<tr>
<td>$A_{on}$</td>
<td>0.104167 mJ/A</td>
</tr>
<tr>
<td>$B_{on}$</td>
<td>350 mJ</td>
</tr>
<tr>
<td>$A_{off}$</td>
<td>0.21875 mJ/A</td>
</tr>
<tr>
<td>Switching</td>
<td></td>
</tr>
<tr>
<td>$B_{off}$</td>
<td>300 mJ</td>
</tr>
<tr>
<td>$k_{Rg, on}$</td>
<td>3.75</td>
</tr>
<tr>
<td>$k_{Rg, off}$</td>
<td>7.5</td>
</tr>
<tr>
<td>$k_{Vce, on}$</td>
<td>1.3333</td>
</tr>
<tr>
<td>$k_{Vce, off}$</td>
<td>1.3333</td>
</tr>
</tbody>
</table>

Table 7 Infineon IGBT module BSM-200-GB-170-DLC parameters

<table>
<thead>
<tr>
<th>IGBT</th>
<th>DIODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction</td>
<td></td>
</tr>
<tr>
<td>$V_{CE,0}$</td>
<td>1V</td>
</tr>
<tr>
<td>$R_t$</td>
<td>10 mΩ</td>
</tr>
<tr>
<td>$A_{on}$</td>
<td>0.102 mJ/A</td>
</tr>
<tr>
<td>$B_{on}$</td>
<td>27.5 mJ</td>
</tr>
<tr>
<td>$A_{off}$</td>
<td>0.24 mJ/A</td>
</tr>
<tr>
<td>Switching</td>
<td></td>
</tr>
<tr>
<td>$B_{off}$</td>
<td>20 mJ</td>
</tr>
<tr>
<td>$k_{Rg, on}$</td>
<td>1.3333</td>
</tr>
<tr>
<td>$k_{Rg, off}$</td>
<td>1.3333</td>
</tr>
<tr>
<td>$k_{Vce, on}$</td>
<td>1.3333</td>
</tr>
<tr>
<td>$k_{Vce, off}$</td>
<td>1.3333</td>
</tr>
</tbody>
</table>

Table 8 presents the calculated total average losses of the DPAB and SPDC topologies, considering the two different operation phases: pulsing and charging. We observe that the DPAB has much higher losses, which mostly come from the charging phase. A detailed explanation of this result is presented in 3.4.

Table 8 DPAB and SPDC topologies average losses

<table>
<thead>
<tr>
<th>TOPOLOGY</th>
<th>Pulsing Losses</th>
<th>Charging Losses</th>
<th>Total Losses</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPAB</td>
<td>2000 W</td>
<td>23164 W</td>
<td>25164 W</td>
</tr>
<tr>
<td>SPDC</td>
<td></td>
<td>8453 W</td>
<td></td>
</tr>
<tr>
<td>Bouncer</td>
<td>633 W</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>FVC</td>
<td>-</td>
<td>7820 W</td>
<td></td>
</tr>
</tbody>
</table>
3.4 Selection and Conclusion

We observe that the losses in the DPAB are three times higher than with SPDC solution, even though the switching frequency during the charging process has been lowered from 20 kHz to 5 kHz, while in the SPDC case a switching frequency of 20 kHz was maintained during both pulsing and charging operation phases. This is a consequence of the fact that the DPAB must be dimensioned in order to withstand the pulse operation ratings (i.e. modulator primary current). This implies that, even though the charging current is very low, the current ratings required during the pulse are high and impose the selection of high power semiconductors. Because these components present higher switching losses than the lower power ones, the efficiency of the system is reduced. Another drawback of the DPAB topology is the fact that the modulator current cannot be initialized in the output filter inductances before the pulse, because the DPAB must also regulate the charging voltage. As a consequence, the current step-up transient is slow. Special care must be taken in the selection of the DPAB output filter capacitance in order to prevent its violent discharge to negative values, because when the main switch closes, all the primary current will flow through it. A final drawback would be the fact that, due to the voltage drop in the transformer during the pulse, it is not possible to perfectly regulate, at the same time, the output and the charging voltages. This solution would be, thus, only interesting when the charging current and the primary currents are closer, which could be the case of long pulse modulators using step-up transformers with low transformation ratios.

On the other hand, the SPDC requires two different power converters to split the output voltage and the charging voltage compensation tasks: an Active Bouncer and a Fast Voltage Corrector (FVC), respectively. By using an individual power converter for each of the compensation tasks, the drawbacks of the DPAB solution are suppressed: the FVC can use low power semiconductors (leading to lower switching losses), the current in the active bouncer inductances can be initialized before the pulse because the two functionalities are now decoupled, and finally the voltage drop in the transformer is not an issue any more to regulate the power fluctuation.

With the different average losses of the two topologies, and considering that CERN pays 0.06 CHF per kWh and that a total of 1638 klystron modulators will be required for CLIC, the operational costs of each topology can be calculated. The DPAB based modulators losses during operation would cost 21.6 MCHF per year (considering 24h operation non-stop), while the SPDC based modulators losses would cost 7 MCHF per year. Regarding the selection of the SPDC bouncer topology, the solution where the first stage is in charge of handling the majority of the primary current with high-efficiency, and the second one is used to fine tune the bouncer voltage via a high-bandwidth low-current linear power converter, is retained. The reason for this choice is not only that the overall efficiency is higher, but also because the utilization of the linear power converter does not
introduce high frequency harmonics (>100 kHz), which cannot be compensated via low level RF (LLRF) closed-loop feedback control [98].

As a conclusion to this chapter, we can state that objectives have been fulfilled, and two new possible droop and power compensator topologies fulfilling CLIC specifications have been successfully identified. It has been demonstrated that the SPDC solution is better suited for the CLIC specific application, as it achieves better efficiency and performances. The following chapter will present the method adopted to optimally dimension the retained solution.
4 DESIGN METHODOLOGY

4.1 Modulator and SPDC design challenge

The design methodology has to take into account that the dimensioning of various modulator components has a very important influence in the active bouncer and fast voltage compensator requirements in order to achieve the same levels of performance. This is illustrated on figure 61: for instance by reducing the size of the main capacitor bank, we reduce the voltage droop that must be compensated by the active bouncer, reducing its large signal requirements. However, this option increases the physical size of the capacitor bank and the total stored energy. In a similar way, the active bouncer requirements will also vary according to the pulse transformer characteristics. If the voltage droop across the transformer windings increases, it will be necessary to increase the active bouncer output voltage ratings and/or the size of the main capacitor bank.

For a specified acceptable level of power fluctuation on the grid, there is also a trade-off to adopt between the FVC dynamics specifications and the bandwidth of the high voltage capacitor charger.

To assess these design problems, several iterative simulations have been carried out to study the influence of the preceding parameters on the overall modulator performances. The results from these simulations considering the CLIC specifications are presented in the following subsections.
4.1.1 Influence of the High Voltage Capacitor Charger Bandwidth

As a starting point to study the bandwidth requirements for the high voltage capacitor charger and the active bouncer, a simulation model composed of an ideal transformer model with a primary voltage of 10 kV and an active bouncer DC-Bus voltage of 1 kV was selected. The main capacitor bank size was dimensioned considering a total drop of 1600 V in the main capacitor bank during the pulse, taking into consideration the technology limitations regarding the switching frequency, and the voltage and current ratings of the active bouncer.

Simulation based sweeps were performed on an active bouncer bandwidth range between 10 kHz and 500 kHz with 5 kHz steps, and on a high voltage capacitor charger bandwidth range between 500 Hz and 10 kHz with 500 Hz steps. The active bouncer and the capacitor charger were modelled as ideal voltage and current sources, respectively, and second order critically damped filter was used to impose a given bandwidth to the ideal references of these sources, as shown on figure 62.

Figure 62: Simulation model used for sweeping bandwidths effects

Figures 63 and 64 show the evolution of the output voltage stability and the power fluctuation, respectively.
Figure 63 Voltage fluctuation vs Active Bouncer and Capacitor charger bandwidths

Figure 64 Power Fluctuation vs Active Bouncer and Capacitor charger bandwidths
From these graphs, we observe that the active bouncer bandwidth presents the most important impact on system performances in terms of output voltage stability and power fluctuation. The high voltage capacitor charger bandwidth also seems to have an important effect up to a frequency of 1.5 kHz to 2 kHz. In the higher frequency range, a charger bandwidth increase introduces very little improve on the modulator performances in terms of output voltage stability and power fluctuation.

### 4.1.2 Influence of main capacitor bank size

Several iterative simulation sweeps have also been performed to quantify the influence of the main capacitor bank $C_m$ size on the Active Bouncer and FVC requirements. A fixed bandwidth of 800 Hz has been imposed for the high voltage capacitor charger. Figures 65 and 66 show the results of these simulations in terms of output voltage fluctuation and power fluctuation, respectively. We can observe that, by increasing by 22% the size of the main capacitor bank (from 225 µF to 275 µF), to achieve an output voltage fluctuation of 1 kV and 10% of power fluctuation, the active bouncer and FVC bandwidths requirements can be reduced from 100 kHz to 60 kHz, respectively.

Figure 65 Capacitor bank size and Active Bouncer bandwidth impact on output voltage fluctuation
4.1.3 Influence of transformer droop

Another parameter that can have an important influence in the active bouncer requirements is the voltage drop across the transformer windings during the pulse. In order to study its effect, the transformer is simulated using a simple circuit containing the equivalent transformer windings resistance and magnetizing inductance of the step-up transformer. The increase of the transformer voltage drop during the pulse is obtained by reducing its magnetizing inductance value. Figures 67 shows the respective influences of the transformer voltage drop during the pulse and of the active bouncer bandwidth on the output voltage fluctuation. To compensate an increasing transformer droop, the Active Bouncer DC bus voltage or the main capacitor bank must be increased. However one can notice that even low bandwidth active bouncer is sufficient to perform this task, as the Active Bouncer bandwidth seems to have very little influence.
4.1.4 Conclusion on the design problem

The simultaneous influence of multiple parameters associated to different modulator subcomponents has been pointed out. The different trade-offs between the specifications and performances of the modulator subcomponents have been clearly identified. An adequate design approach able to cope with this complexity has to be adopted, in order to optimally dimension a modulator fulfilling the CLIC specifications. In addition, as introduced in chapter one, simultaneous R&D studies were simultaneously carried out on CLIC electrical interface with the 400 kV grid and the klystron tube itself. In order to quickly evaluate the impact on the modulator design of changes on specifications or new design choices on these two topics, a generic and versatile dimensioning tool must be developed.
4.2 Method Description

According to the challenges previously presented, a clear methodological approach has been developed. Its structure is illustrated on figure 68, which includes the different tasks and tools that have been developed and used in this thesis. They will be presented in the following chapters.

This first step consists in the research and identification of appropriate power converter topologies, able to make a monolithic pulse transformer-based modulator operate at constant power consumption and, at the same time, respect CLIC output pulse and efficiency specifications. The results of this study have been already presented in chapter 3.

In a second step, a Power Electronics System Dimensioning Tool integrating several power converters dimensioning or design models based on analytical expressions, has been developed. Some of the dimensioning models included are:

- Semiconductor losses design tool.
- Cooling system design tool.
- Inductance design tool.
- Control design tool.

These models are described in detail in chapter 5.

As a third step, the system dimensioning tool is used to evaluate the power converter topology candidates and make a topology choice. Afterwards the design models are verified experimentally by constructing reduced-scale prototypes, which are also used to validate the operation of the proposed topologies. Chapter 6 describes in detail the different experimental validation set-ups and results.

After the validation of the design models, the Power Electronics System Design Tool is integrated into a global optimal design environment. This optimal design environment is used to optimally dimension a full-scale modulator respecting the CLIC specifications. Chapter 7 describes in detail the optimization procedures and the final dimensioning of the CLIC klystron modulator.
When considering the need of an integrated design approach, the difficulty lies in the determination of the optimal compromise between design models accuracy and time to achieve results. Looking at figure 68 one appreciates the extent of this work, spanning from topologies selection to full power system construction and validation. It is clear that the effort in this work will be predominantly put into the integration of existing models (e.g. thermal) into an efficient design environment. However, due to the extremely challenging performances required, specific models/methods have to be extensively developed. Particularly, the topological research and the development of the associated control methods are central tasks in this work.

As presented in 4.1, the design of the CLIC klystron modulator requires an integrated system approach considering all the modulator subcomponents into a design optimization environment. Different strategies and ways of using optimization methods to optimize power converter designs have been studied and proposed during the last 30 years. Several solutions in the literature proposed different methods to maximize the robustness and the efficiency, or minimize weight, volume and cost, by modifying whether the control parameters or directly the power converter design. Typical optimization procedures are based on Genetic Algorithms (GAs) [99][100][101], Augmented Lagrangian (ALAG) [102][103][104], and Sequential quadratic programing (SQP) [105].
In order to speed-up the computation time, the design models are usually based on analytical formulation. Moreover, the designer also introduces simplifications and design constraints from previous design experience. As a consequence, their accuracy is reduced in comparison with simulation-based optimization techniques, which make possible to easily consider delays, saturations, and other nonlinearities present in the real system. However, the important computation time required for performing a numerical simulation on every optimization step/iteration, usually forces the designer to reduce the optimization variables to a reduced subset. As an alternative, in order to achieve a trade-off between design time and accuracy, in this thesis it has been decided to use a hybrid optimal design methodology using Space Mapping techniques that has been previously successfully proposed and used in the literature to efficiently optimize electrical machines considering magnetic saturation effects [106].

This approach uses models with different levels of complexity. The first model, or “coarse model”, is very light in terms of computing time but less accurate. The second model, or “fine model” is much more accurate, but computationally much more heavy. The proposed method, illustrated on figure 69, utilizes the coarse model to perform nonlinear optimization techniques, and the fine model to verify, validate and improve the results obtained using the coarse model.

The implantation of this dimensioning method begins by selecting a power converter topology, setting the optimization objectives in terms of minimum performances that must be respected (constraints), the performance or parameters that must be optimized (e.g. bandwidth, efficiency, etc.), and selecting the optimization variables (controller parameters only or/and power stage component values). Then, after an initialization of the optimization variables, which are set thanks to the designer expertise, a first optimization routine starts, where the performances are evaluated using analytical design models (they will be presented in chapter 5). Once an optimal solution is obtained, a time-domain simulation with the calculated parameters is carried out. If differences are found between the analytically predicted performances and the ones obtained in the numerical simulation, the frequency-domain models are modified/corrected via correction factors, and the optimization routine is
restarted again. It has been proved that, after a limited number of corrective iterations, the analytical and numerical model converge. At the end of the whole procedure, illustrated in figure 70, the final optimal solution is naturally numerically validated. It is interesting to note that during the optimization procedure the corrective factors for the analytical model can be saved at each corrective iteration. This allows the designer to appreciate the exactness of the initial analytical model and the evolution in its correction. This method offers a good compromise between the speed of the analytical model-based optimization approach and, at the same time, achieving the same accuracy of the time-domain numerical simulation-based models.

Figure 70 Proposed Hybrid optimization scheme
CHAPTER V

5 DESIGN MODELS AND VALIDATION

5.1 Semiconductors Losses

The calculation of semiconductor losses can be addressed in three different ways. The first approach consists of a physics-based finite element analysis simulation. Results using this method match the experimental results very well but the computation time is too long (the simulation of a few switching cycles can take several days using computing workstations). The second approach consists of behavioral model-based simulation. These models, such as PSPICE or SABER (almost every vendor provides these kinds of device behavior models), describe the device behavior as a function of some key parameters. This method provides a good trade-off between accuracy and simulation time, however the simulation time is still high to be used in an efficient global optimization tool. The third approach is the analytical model. This last method is the fastest and most suitable for data processing. It can be addressed with different levels of complexity, in order to improve its accuracy. The basic models and several improvements proposed in the literature to increase its accuracy will be reviewed hereafter.

The total power semiconductor losses are the sum of the conduction losses, the switching losses and the blocking losses, as shown on (13). The blocking losses are usually neglected, as only a leakage current in the nA level flows through the collector-emitter terminals (the computation of these losses would be similar to the computation of the conduction losses).

\[
P_{\text{losses}} = P_{\text{conduction}} + P_{\text{switching}} + P_{\text{blocking}} \approx P_{\text{conduction}} + P_{\text{switching}} \tag{13}
\]
5.1.1 Power Switch Losses

5.1.1.1 IGBT Conduction Losses

The conduction losses can be computed using the known expression (14), being $T_{sw}$ the inverse of the switching frequency, $I_c$ the current flowing through the semiconductor and $V_{CE_{sat}}$ the semiconductor saturation voltage:

$$P_{cond} = \frac{1}{T_{sw}} \int_0^{T_{sw}} (I_c V_{CE_{sat}}) \, dt$$  \hspace{1cm} (14)

However, in an IGBT the saturation voltage changes as a function of the current flowing through the IGBT, $I_c$, and it also depends on the junction temperature, $T_j$, as depicted on figure 71.

The saturation voltage is often modelled with a first order approximation\(^6\), considering a threshold voltage $V_{CE_0}$ and a dynamical resistance, $r_t$, as shown in (15).

$$V_{CE_{sat}} = V_{CE_0} + I_c r_t$$  \hspace{1cm} (15)

\(^6\) In the design tools, the highest temperature curve from the $V_{CE} - I_c$ curve provided by the IGBT manufacturer has been modelled, as a conservative approach.

Figure 71 Change on $V_{CE}$ as a function of $I_c$ and $T_j$ for a SEMIX 356GB126HD Trench IGBT module
Introducing equation 15 on equation 14, we obtain the conduction losses as a function of the average and RMS current flowing through the IGBT, as shown in (16)

\[
P_{cond} = \frac{1}{T_{sw}} \int_0^{T_e} (I_c(V_{CE,0} + I_c r_c))dt = \frac{1}{T_{sw}} \int_0^{T_e} (I_c V_{CE,0})dt + \frac{1}{T_{sw}} \int_0^{T_e} (I_c^2 r_c)dt = \\
\frac{V_{CE,0}}{T_{sw}} \int_0^{T_e} (I_c)dt + \frac{r_c}{T_{sw}} \int_0^{T_e} (I_c^2)dt = V_{CE,0} I_{Av} + r_c I_{RMS}^2
\]

(16)

Considering that we can have three different current waveforms when switching an IGBT with square-wave voltage output: rectangular, trapezoidal and triangular (see figure 72); solving equation 16 we obtain the expression of the conduction losses for each of the waveforms respectively.

A)  
\[
P_{cond} = \frac{1}{T_{sw}} (V_{CE,0} I_c + I_c^2 r_c) I_{on}
\]

(17)

Current waveform B:

\[
P_{cond} = \frac{1}{T_{sw}} (V_{CE,0} \frac{I_{c(1)} + I_{c(2)}}{2} + r_c (\frac{I_{c(1)}^2}{3} + I_{c(2)}^2 + I_{c(1)} I_{c(2)})) I_{on}
\]

(18)

Current waveform C:

\[
P_{cond} = \frac{1}{T_{sw}} (\frac{I_{c(1)}}{6}(3V_{CE,0} + 2 I_c r_c)) I_{on}
\]

(19)

Figure 72 Possible I_c waveforms

Current waveform A:

\[
P_{cond} = \frac{1}{T_{sw}} (V_{CE,0} I_c + I_c^2 r_c) I_{on}
\]

Current waveform B:

\[
P_{cond} = \frac{1}{T_{sw}} (V_{CE,0} \frac{I_{c(1)} + I_{c(2)}}{2} + r_c (\frac{I_{c(1)}^2}{3} + I_{c(2)}^2 + I_{c(1)} I_{c(2)})) I_{on}
\]

Current waveform C:

\[
P_{cond} = \frac{1}{T_{sw}} (\frac{I_{c(1)}}{6}(3V_{CE,0} + 2 I_c r_c)) I_{on}
\]
In order to verify the precision of the $V_{CE, sat}$ values specified by the manufacturers of the power switches in their datasheets, intensive measurements on two different IGBTs (1600 V technology, 200 A Semikron 195GB066D; and a 1700 V technology, 450 A SEMIX 653GAR176HDs) were performed. The electrical circuit for this test consisted directly into an oversized capacitor bank (20mF), and a low-inductive resistive load. As shown on figure 73, $V_{CE, sat}$ decreases with time at the beginning of the conduction phase, achieving a final steady-state value after approximately 60 µs. This time length would correspond to a complete pulse at a switching frequency of 16 kHz. As likely even faster switching frequencies will be required for CLIC application, intensive measurements at faster switching pulse times were performed. Figures 74 and 75 show the experimental results obtained for different pulse lengths using a 600 V and a 1700 V IGBT, respectively.

Figure 73 Switching waveforms: IGBT $V_{CE}$ in yellow; IGBT current in blue; and IGBT gate voltage in purple.
Figure 74 $V_{CE\_sat}$ values for different pulse lengths on a Semikron 600V IGBT 195GB066D

Figure 75 $V_{CE\_sat}$ values for different pulse lengths on a SEMIX653 1700V IGBT
From these figures we observe that the datasheet values correspond to the $V_{CE_{sat}}$ value after an 80 $\mu$s pulse. Additional tests were performed with inductive load, reducing the resistance load instead of varying the DC-bus voltage to increase the current flowing through the semiconductor. The $V_{CE_{sat}}$ voltage waveform did not experience changes by changing these parameters. The ambient temperature during all tests remained between 21ºC and 22ºC.

In order to improve the accuracy of the conduction losses estimation, this thesis proposes an improved expression including a new factor $k_f$ to introduce the influence of the switching frequency in the computation of the conduction loss.

$$V_{CE_{sat}} = V_{CE_{0}} + k_f I_c r_f$$

(20)

Where the frequency factor can be calculated as the relation between the average saturation voltage at the user switching frequency and the saturation voltage provided by the data sheet, both at the switch nominal current, as shown in 21.

$$k_f = \frac{V_{CE_{sat_{-user}}}}{V_{CE_{sat_{-datasheet}}}}$$

(21)

The classical switching loss prediction expression is a good approximation; however it lacks accuracy during the quasi-saturation region of the switch. The switching waveform is also strongly influenced by the power provided by the IGBT driver during commutations, parasitic inductances of the IGBT module itself and its connection to the DC bus, external snubber circuits, etc. The proposed factor allows to consider the effects of these factors experimentally to improve the conduction loss prediction.

An alternative to improve the accuracy of the classical conduction loss calculation comes from the fact that saturation voltage with the switching current is closer to a second order polynomial than to a straight line. Therefore, a different expression consisting in fitting with a second order polynomial the instantaneous power dissipated in the switch as a function of the switch current is proposed. The improved accuracy of the new expression is illustrated by plotting the instantaneous power as a function of the current for the same previous 600V and 1700V IGBT switches, shown in figures 76 and 77 respectively.
Figure 76 Instantaneous power values for different pulse lengths on a Semikron 600V IGBT 195GB066D

Figure 77 Instantaneous power values for different pulse lengths on a SEMIX653 1700V IGBT
5.1.1.2 IGBT Switching Losses

In a power switch, the transition from blocking to saturation and vice versa is not instantaneous, and therefore energy is dissipated during these transitions; as illustrated in figure 78.

![Switching waveforms on a power switch during: A) Turn on; B) Turn-off](image)

The switching losses can be ideally calculated using the following expression:

\[
P_{sw} = \frac{1}{T_{sw}} (E_{on} + E_{off}) = \frac{1}{T_{sw}} \left( \int_{0}^{t_{on}} (V_{CE}(t) \cdot I(t)) dt + \int_{0}^{t_{off}} (V_{CE}(t) \cdot I(t)) dt \right)
\]  

(22)

However, in order to use this expression the evolution of \(V_{CE}\) and \(I_{c}\) during the switching transitions has to be perfectly known. Due to the fact that the switching waveforms depend on the load characteristics and gate driving conditions, in order to achieve good accuracy, this method has to be approached by experimental measurement for every switching set-up.

No simple expression can be found for the voltage and current during a switching transient. Instead, the IGBT suppliers provide the values of the turn on and turn off energies as a function of the current flowing through the power switch and the gate resistance, for a given switching voltage, dice temperature, and gate driving voltage; as shown in figures 79 and 80.
Figure 79 Turn-on and turn-off energy as a function of $I_C$ on a SEMIX 252GB176HD IGBT

Figure 80 Turn-on and turn-off energies as a function of $R_G$ on a SEMIX 252GB176HD IGBT
With the purpose of simplifying the analysis of the switching losses for different current levels, the energy loss curves can be approximated as a function of $I_C$ by linear interpolation\(^7\), as follows [136][137][138]:

$$E_{on} = A_{on} \cdot I_C + B_{on}$$  \hspace{1cm} (23)

$$A_{on} = \frac{\Delta E_{on}}{\Delta I_C} = \frac{E_{on(2)}-E_{on(1)}}{I_{C(2)}-I_{C(1)}}$$  \hspace{1cm} (24)

$$B_{on} = E_{on(2)} - A_{on} \cdot I_{C(2)}$$  \hspace{1cm} (25)

$$E_{off} = A_{off} \cdot I_C + B_{off}$$  \hspace{1cm} (26)

$$A_{off} = \frac{\Delta E_{off}}{\Delta I_C} = \frac{E_{off(2)}-E_{off(1)}}{I_{C(2)}-I_{C(1)}}$$  \hspace{1cm} (27)

$$B_{off} = E_{off(2)} - A_{off} \cdot I_{C(2)}$$  \hspace{1cm} (28)

In order to evaluate the influence of the gate resistance and $V_{CE}$ voltage values for each application, expressions (23) to (26) must be adapted using scale factors. The gate resistance factors, $k_{RG_{on}}$ and $k_{RG_{off}}$, can be calculated from the switching energies graph of figure 74, taking into account the value of the gate resistance specified in the datasheet, $R_{GDS}$, and the one used on the specific application, $R_{GUSER}$, as specified in (29) and (30).

$$k_{RG_{on}} = \frac{E_{on}(R_{GUSER})}{E_{on}(R_{GDS})}$$  \hspace{1cm} (29)

$$k_{RG_{off}} = \frac{E_{off}(R_{GUSER})}{E_{off}(R_{GDS})}$$  \hspace{1cm} (30)

The $V_{CE}$ voltage influences almost only in a linear way the energy dissipated during the switching transitions. Therefore, the voltage scaling factors can be calculated as a function of the $V_{CE}$ voltage during the blocking state specified in the datasheet, $V_{CE_{DS}}$, and the actual voltage in a specific application, $V_{CE_{USER}}$. Equations (31) and (32) show the calculation of these factors, where $V_{CE_{on}}$ and $V_{CE_{off}}$ are the values of the $V_{CE}$ voltage before and after the on and off switching transitions, respectively (these values will usually be slightly different, particularly for capacitor bank discharge based applications).

---

\(^7\) Please note that, as a simplification, no DC bus voltage change is considered during operation due to the discharge of the capacitor bank.
\[ k_{V_{CE-on}} = \frac{V_{USER}}{V_{DS}} \]  \hspace{1cm} (31)

\[ k_{V_{CE-off}} = \frac{V_{USER}}{V_{DS}} \]  \hspace{1cm} (32)

As previously performed for the conduction losses calculation, taking now into account the possible \( I_c \) waveforms of figure 72, the switching losses can be calculated by the following expressions:

Current waveform A:

\[ P_{SW} = \frac{1}{T_{SW}} (E_{on} + E_{off}) = \]

\[ = \frac{1}{T_{SW}} \left( (A_{on} \times I_c + B_{on}) \cdot k_{R_{G-on}} \cdot k_{V_{CE-on}} + (A_{off} \times I_c + B_{off}) \cdot k_{R_{G-off}} \cdot k_{V_{CE-off}} \right) \]  \hspace{1cm} (33)

Current waveform B:

\[ P_{SW} = \frac{1}{T_{SW}} (E_{on} + E_{off}) = \]

\[ = \frac{1}{T_{SW}} \left( (A_{on} \times I_c(1) + B_{on}) \cdot k_{R_{G-on}} \cdot k_{V_{CE-on}} + (A_{off} \times I_c(2) + B_{off}) \cdot k_{R_{G-off}} \cdot k_{V_{CE-off}} \right) \]  \hspace{1cm} (34)

Current waveform C:

\[ P_{SW} = \frac{1}{T_{SW}} (E_{on} + E_{off}) = \frac{1}{T_{SW}} \left( 0 + (A_{off} \times I_c + B_{off}) \cdot k_{R_{G-off}} \cdot k_{V_{CE-off}} \right) \]  \hspace{1cm} (35)
5.1.2 Diode Losses

The losses in a power diode can be calculated as the sum of the conduction losses plus the reverse-recovery losses. The diode turn-on energy and the losses due to the leakage current during the blocking state can be neglected.

5.1.2.1 Diode Conduction Losses

The conduction losses as a function of the forward voltage and current during a cycle can be calculated using the classical expression:

\[
P_{\text{cond,diode}} = \frac{1}{T_{\text{sw}}} \int_{0}^{T_{\text{sw}}} (V_F(t) \cdot I_F(t)) \, dt
\]  

(36)

The diode forward voltage can be approximated by a first order approximation, as shown in figure 81, in the same way as previously did in 5.1.1.1 for the power switch:

\[
V_F = V_{F0} + R_D \cdot I_F
\]  

(37)

Figure 81 Diode forward voltage as a function of the forward current \(I_F\)
Applying this approximation in (36), we calculate the general expression of the conduction losses in the diode:

\[
P_{\text{cond,diode}} = \frac{1}{t_{\text{sw}}} \int_0^{t_{\text{sw}}} \left( V_{F0} * I_F(t) + R_D * I_F^2(t) \right) \, dt = V_{F0} * I_{F,AV} + R_D * I_{F,RMS}^2
\]  

(38)

Solving this equation for the three possible current waveforms previously depicted on figure 72, we obtain:

Current waveform A:

\[
P_{\text{cond,diode}} = \frac{1}{t_{\text{sw}}} (V_{F0} * I_F + I_F^2 * R_D) * t_{\text{on}}
\]  

(39)

Current waveform B:

\[
P_{\text{cond,diode}} = \frac{1}{t_{\text{sw}}} \left( V_{F0} \frac{I_{F(1)}+I_{F(2)}}{2} + \frac{1}{3} R_D (I_{F(1)}^2 + I_{F(1)} I_{F(2)} + I_{F(2)}^2) \right) * t_{\text{on}}
\]  

(40)

Current waveform C:

\[
P_{\text{cond,diode}} = \frac{1}{t_{\text{sw}}} \left( \frac{5}{6} I_F (3 * V_{F0} + 2 * I_F * R_D) \right) * t_{\text{on}}
\]  

(41)

5.1.2.2 Diode Reverse Recovery Losses

The specific data provided for calculating the diode reverse-recovery losses differs from one manufacturer to another. The reverse recovery losses depend on the current slope during the transition, which is determined by the inductance of the circuit and the complementary power switch \( \frac{dI}{dt} \) during turn-on. Usually the reverse-recovery energy, \( E_{rr} \), is specified in the datasheet only for one operating point, and the reverse-recovery energy can be adapting using a scale factor \( k_{rr} \):

\[
k_{rr} = \frac{E_{rr}^{DS}}{E_{rr}^{DS}} \cdot \frac{Q_{rr}^{DS}}{Q_{rr}^{DS}}
\]  

(42)
Where $E_{rr}^{DS}$, $Q_{rr}^{DS}$ and $V_{CE}^{DS}$ are the reverse-recovery energy, reverse-recovery charge and voltage specified in the datasheet, respectively.

The total reverse-recovery losses are estimated by using the following general expression:

$$P_{RR} = \frac{1}{T_{sw}} \left( k_{rr} \cdot Q_{rr}^{USER} \cdot V_{CE}^{USER} \right) = \frac{1}{T_{sw}} \left( k_{rr} \cdot \frac{I_{rr} \cdot t_{rr}}{2} \cdot V_{CE}^{USER} \right)$$  \hspace{1cm} (43)

The analytical models presented in this section 5.1 have been integrated in the Semiconductor losses design model of the Power Electronics System Design tool, as previously explained during the methodology explanation of chapter 4, and illustrated on Figure 68. The specific implementation of these models into the tool will be further explained in chapter 7.

5.1.3 Linear operation losses

The particular case of operating the semiconductors in the linear or ohmic region, which applies to the linear stage of the SPDC topology presented in 3.2.4, is explained hereafter. The losses when operating a power switch in the active region $P_{LL}$, are the sum of the power dissipated in the semiconductor $P_{SLL}$ plus the driving losses $P_{drive}$, as shown on (44).

$$P_{LL} = P_{SLL} + P_{drive}$$  \hspace{1cm} (44)

The MOSFET technology with extended forward bias safe operating area for linear operation, intended to use for the linear stage has maximum values of gate-source capacitance of 250 nC, and internal gate resistance of 3.5 $\Omega$. This implies that for the specific case of CLIC pulse width and repetition rate, the driving losses are below 5 mW average, and therefore can be neglected. The semiconductor linear loss $P_{SLL}$, can be calculated as the multiplication of the average current passing through the linear stage by the average voltage drop during the modulator pulse, as shown in the following expression:

$$P_{SLL} = \frac{1}{T} \left( V_{DC_{bus}} - \frac{V_{bouncer}}{2} \right) \frac{I_{DS}}{2}$$  \hspace{1cm} (45)
Where $V_{DC,\text{bus}}$ is the linear stage DC bus voltage, $V_{\text{bouncer}}$ is the voltage droop compensated by the active bouncer, and $I_{DS}$ the average current passing through each MOSFET during the modulator pulse. The voltage discharge experienced in the linear stage DC bus voltage during the pulse has been neglected in this expression.

5.2 Cooling

The losses calculation can be used to estimate the power switch maximum, minimum and average temperature for a given heat sink material and geometry. This information can also be used to estimate the power switch lifetime, which could be reduced because of thermal cycling. The calculation of these parameters will be explained hereafter in four different subsections: general thermal model, heat sink parameters extraction, analytical computation of junction temperature, and IGBT lifetime estimation.

5.2.1 Thermal equivalent model

The time evolution of the temperature for a given system is defined by the source of dissipation and the thermal impedance of the system. Power switch manufacturers normally express the thermal impedance of a specific switch using two different forms: Foster and Cauer. The Foster model has the analytical form described in (46), where each $R$ and $C$ values are not real parameters related to the power switch semiconductor layers, but just fitting coefficients calculated to approach with a function the experimentally measured impedance. Figure 82 shows a typical Foster IGBT model with 4 pairs of RC time constants.

$$Z_{th} = \sum_{i=1}^{N} R_i \cdot (1 - e^{\frac{t}{\tau_{i,li}}})$$  (46)
Using the Foster form, it is possible to connect all components involved in the thermal circuit, namely thermal paste and heat sink, as illustrated on Figure 83. The limitations of this model come from the fact that the thermal impedance of each component is normally identified independently, and the RC time constants are connected in series, instead of having a reference point to ground. As a consequence it is not possible to evaluate the transient evolution of a temperature in one node of the circuit, but only the steady-state temperature.

In order to evaluate the transient evolution of the temperature on every node of the circuit, it is possible to calculate an equivalent thermal model where each thermal capacitance is reference to ground. This more coherent thermal model in terms of physics is known as Cauer form, and it is illustrated on Figure 84.
The iterative procedure to calculate the Cauer canonical form from the Foster canonical form is a well-known iterative procedure [107]. Due to the fact that during the optimization procedure the only point that is evaluated in dynamics is the evolution of the junction temperature (in order to evaluate possible thermal cycling effects), the Foster model is retained in order to simplify all the calculations.

The power switch manufacturers normally express the thermal impedance of the switch as four pairs of Foster parameters for the switch itself, and an additional set of four parameters for its associated diode, as shown on figures 85 and 86, respectively.
The complete Foster equivalent thermal circuit considering the presence of both elements, power switch and diode, on a power module, is shown on figure 87.
5.2.2 Steady-state thermal calculation method

Several thermal calculations are required to verify that the maximum junction temperature inside the power switches and diodes is not exceeded during operation, which would lead to device destruction. However, due to the 50Hz pulsed operation CLIC requires, it is also important to evaluate the effect of thermal cycling on power switches lifetime. In order to compute the junction temperature swing $\Delta T$ in steady-state, normally numerical simulations with very long simulation time are required until the system reaches a steady-state thermal oscillation. Due to the fact that in this thesis this evaluation has to be performed for every iteration step of the non-linear optimization procedure, reduce computation time is a must. In order to speed-up the calculation of the steady-state temperature swing, a frequency domain solver method based on the Fourier convolution theorem (47) is proposed.

$$F\{f * g\} = F\{f\} \cdot F\{g\} \quad (47)$$

In this expression, we can consider $f$ is the excitation function, i.e. the semiconductor power losses steady-state cycle, and $g$ the thermal impedance of the cooling system. By applying the inverse Fourier transform, we arrive to:

Figure 87 Complete power module Foster thermal equivalent circuit
This equation states that the steady-state time-domain solution of the thermal system \( g \) exposed to a thermal excitation or power loss function \( f \), which is equivalent to the time-domain convolution of the two functions, can be computed in a more simple way in the frequency domain by calculating the inverse Fourier transform of the product of the individual Fourier transforms of the two functions. The proposed frequency-domain solver method is illustrated on figure 88. The different functions can be calculated analytically beforehand with some simplifying assumptions. With such an approach, each iteration of the optimization procedure can be computed very rapidly, without the need of using long numerical simulation tasks.

![Figure 88 Thermal steady-state computation based on a frequency domain solver](image)

The particular application of this method to the specific CLIC application is explained hereafter. For the sake of simplicity, the case of a single switch, illustrated on figure 82, will be considered.

The power loss function can be modeled as a train of pulses with pulse width \( t_{\text{pulse}} \) and power loss amplitude \( A \), corresponding to the average power loss during the pulse in the switch, with a period \( T_0 \) of 20 ms (50 Hz operation), as shown on figure 89.
The train of pulses can be mathematically described by a Fourier series:

$$f(t) = \sum_{k=-\infty}^{+\infty} \left[ \frac{A}{\pi k} \sin\left(\pi \frac{t_{flat}}{T_0} \frac{k}{T_0} \right) \cdot e^{jak \omega_0 t} \right]$$

$$= \sum_{k=1}^{+\infty} \left[ \frac{A}{\pi k} \sin\left(\pi \frac{t_{flat}}{T_0} \frac{k}{T_0} \right) \left( e^{jak \omega_0 t} - e^{jak \omega_0 t} \right) \right]$$

(49)

Applying the Fourier transform to the Fourier series, we obtain:

$$F[f(t)] = \sum_{k=1}^{+\infty} \left[ \frac{2A}{k} \sin\left(\pi \frac{t_{flat}}{T_0} \frac{k}{T_0} \right) \cdot \left( \delta(\omega - k \omega_0) + \delta(\omega + k \omega_0) \right) \right]$$

(50)

The thermal impedance of figure 82 can be described by the following thermal transfer function (49) and its corresponding Fourier transform (50).

$$G(s) = \sum_{l=1}^{6} \left[ \frac{R_i}{1 + R_c C_i s} \right]$$

(51)

$$G(j\omega) = \sum_{l=1}^{6} \left[ \frac{R_i}{1 + R_c C_i j\omega} \right]$$

(52)

Having already the individual Fourier transform of the power loss function and the thermal impedance, their product is given by (53).

$$T(\omega) = \sum_{k=1}^{+\infty} \left[ \frac{2A}{k} \sin\left(\pi \frac{t_{flat}}{T_0} \frac{k}{T_0} \right) \cdot \left( \delta(\omega - k \omega_0) + \delta(\omega + k \omega_0) \right) \right] \cdot \sum_{l=1}^{6} \left[ \frac{R_i}{1 + R_c C_i j\omega} \right]$$

(53)
Computing the inverse Fourier transform of (53), we obtain the steady-state time-domain solution:

\[ T(t) = \sum_{k=1}^{+\infty} \left[ \frac{A}{\pi K} \sin \left( \frac{\pi t_{flat} K}{T_0} \right) \right] \left[ \sum_{l=1}^{6} R_i \frac{1}{1+R_i C_l j K \omega_0} e^{j k \omega_0 t} + \frac{R_i}{1-R_i C_l j K \omega_0} e^{-j k \omega_0 t} \right] \]  

(54)

Applying different transformations we can simplify this expression:

\[ T(t) = \sum_{k=1}^{+\infty} \left[ \frac{A}{\pi K} \sin \left( \frac{\pi t_{flat} K}{T_0} \right) \right] \left[ \sum_{l=1}^{6} \frac{R_i}{1+R_i C_l j K \omega_0} \right] \cdot 2. \cos (k \cdot \omega_0, t + \varphi_k) \]  

(55)

Being \( \varphi_k \):

\[ \varphi_k = \arg \left( \sum_{l=1}^{6} \frac{R_i}{1+R_i C_l j K \omega_0} \right) \]  

(56)

Minimum and maximum temperature values occur at \( t = -\frac{t_{flat}}{2} \) and \( t = \frac{t_{flat}}{2} \) respectively, corresponding to the start and finish of the power loss pulse function of figure 89.

Results obtained using expression (55) for different thermal circuits, were compared with numerical simulation results. Figure 90 shows the reduction of the error when increasing the number of harmonics considered for the Fourier series. Figure 91 shows the computation time required to compute the steady-state time-domain solution as a function of the number of harmonics considered for the Fourier series.
Figure 90 Error versus number of Fourier harmonics

Figure 91 Error versus number of Fourier harmonics
As an experimental verification of the accuracy of the previously presented analytical power loss and thermal design models, a mixed test was performed. Using a thermal camera, the case temperature of an IGBT SKM 195GB066D from Semikron was monitored while switching continuously a 100 V DC bus on a 25 Ω resistive load at different switching frequencies with a duty cycle $D = 0.5$. The value final steady-state temperature allows the verification of the conduction and switching average losses calculation, and the accuracy of the considered thermal resistances. On the other hand, the time required to achieve the steady-state temperature makes possible to verify the accuracy of the thermal capacitances.

Figure 92 shows several thermal camera images taken during the tests. The differences between experimental measurements of the steady-state IGBT case temperature and the IGBT case steady-state temperature computed with the proposed analytical method can be observed on figure 93. The steady-state temperature was reached after 45min, and the maximum absolute error between experimental and calculated values in this case remained below 0.2°C.

![Figure 92 Thermal camera images acquired on IGBT temperature experimental set-up](image)
Figure 93 Measured and calculated temperatures on IGBT Semikron SKM 195GB066D
5.2.3 Heat-sink calculation

The heat-sink dimensioning model is used to derive the equivalent thermal resistance and thermal capacitance from the dimensions of a generic heat-sink structure. Figure 94 illustrates the considered geometrical variables defining the heat-sink geometry of the generic heat-sink structure depicted in figure 95. The heat-sink total length and total width, $L_t$ and $W_t$, respectively, define external dimensions of the base-plate. $W_f$ and $W_{if}$ are the fin width and distance between two consecutive fins, respectively. Finally $H_{bp}$ and $H_f$ are the base-plate height and fin height, respectively.

Starting with the heat-sink thermal resistance, the base plate resistance can be computed using the following equation:

$$R_{BP} = \frac{H_{bp}}{k_{Al}L_tW_t}$$  \hspace{1cm} (57)

Where $k_{Al}$ is the thermal conductivity of the heat-sink material (aluminium).

The convection of each fin to air and the conduction effect on each fin can be modelled considering a thermal resistance matrix of $M$ elements [134], as shown on Figure 96, where each thermal conduction and convection resistance is defined as:

$$R_{f,\text{conv}} = \frac{1}{M \cdot h_{\text{conv}} A_f \eta_f}$$ \hspace{1cm} (58)

$$R_{f,\text{cond}} = \frac{H_f}{M \cdot k_{Al} L_t W_f}$$ \hspace{1cm} (59)

Where $A_f$ is the external area of an individual fin, $\eta_f$ is a factor calculated following expression (60), and $h_{\text{conv}}$ is the heat exchange coefficient calculated using the Nusselt number $Nu$ as shown in (61).

$$\eta_f = \frac{\tanh \left( \frac{2 \cdot h_{\text{conv}} H_f}{k_{Al} W_f} \right)}{\sqrt{k_{Al} W_f}}$$ \hspace{1cm} (60)

$$h_{\text{conv}} = \frac{Nu \cdot k_{\text{air}}}{W_{if}}$$ \hspace{1cm} (61)
Figure 94 Heat-sink geometrical variables
Where $k_{\text{air}}$ is the thermal conductivity of the air and $W_f$ the distance between two consecutive fins. The calculation of the Nusselt number can be performed using the expression (62), which is valid for a range of modified Reynolds number between 0.1 and 100.

$$Nu = \left( \frac{1}{\left( \frac{Re^*Pr}{2} \right)^3} + \frac{1}{0.664(Pr)^{1.2}(Re^*+3.65)^{1.2}} \right)^{-1/3}$$  \hspace{1cm} (62)$$

In this expression, $Re^*$ and $Pr$ are the Reynolds modified number and the Prandtl number, respectively. These can be computed with the following expressions:

$$Re^* = \frac{\rho_{\text{air}}V_{\text{air}}W_f^2}{\mu_{\text{air}}L_t}$$  \hspace{1cm} (63)$$

$$Pr = \frac{\mu_{\text{air}}C_p}{k_{\text{air}}}$$  \hspace{1cm} (64)$$

Where $\rho_{\text{air}}$, $V_{\text{air}}$, $\mu_{\text{air}}$, and $C_p$, are the density, the speed, the dynamic viscosity and the specific heat of air respectively.

Figure 95 Generic heat-sink 3D model
Developing the equations (58) and (59), we can compute the total equivalent thermal resistance of a fin:

\[ R_f = -\frac{1}{2} \frac{A(-B)^M R_{f,\text{cond}}(-B)^M + A C M + R_{f,\text{cond}}}{(-B)^M - C^M} \]  

(65)

The parameters A, B, and C being:

\[ A = \sqrt{R_{f,\text{cond}} \cdot (R_{f,\text{cond}} + 4 R_{f,\text{conv}})} \]  

(66)

\[ B = \frac{\sqrt{2 R_{f,\text{conv}} - R_{f,\text{cond}} + A}}{R_{f,\text{conv}}} \]  

(67)

\[ C = \frac{2 R_{f,\text{conv}} + R_{f,\text{cond}} + A}{R_{f,\text{conv}}} \]  

(68)

Considering the total number of fins, \( N_f \), the total heat-sink thermal resistance \( R_{\text{HS}} \) can be calculated as shown in (69).

\[ R_{\text{BP}} = R_{\text{BP}} + \frac{R_f}{N_f} \]  

(69)
The equivalent thermal capacitance of the heat-sink can be directly calculated using the following expression:

\[
C_{HS} = H_{Al} \cdot \rho_{Al} \cdot V_{Al}
\]  

(70)

Where \(H_{Al}, \rho_{Al}\) and \(V_{Al}\) are the aluminium heat capacitance, density and total volume (on base plate and fins).

The heat-sink volume can also be computed from its external dimensions using (71):

\[
V_{HS} = L \cdot W \cdot (H_f + H_{BP})
\]  

(71)

The analytical models presented in this section 5.2 have been integrated in the cooling system design model of the Power Electronics System Design tool, previously introduced during the methodology explanation of chapter 4, and illustrated on Figure 68. The specific implementation of these models into the tool will be further explained in chapter 7.

### 5.3 Power switch lifetime

The failure rate of a power switch is typically represented by a “bathtub curve”, as depicted on figure 97. We distinguish three different phases for failures in time: early failures, random failures and wear-out failures [135].

![Figure 97 Typical failure rate with time on a power module](image-url)
The early failures in power switch modules are caused by manufacturing defects (e.g. cracking on semiconductor layers) or human errors (e.g. ESD on gate and emitter due to touching). The only way to reduce these errors is by quality improvement and correct handling.

Random failures come after early failures. These failures depend on operating conditions which could cause stress of the power module (overvoltage, overcurrent, overheat, etc).

After the random failure area there is the wear-out phase, where failures are caused by wear or fatigue of the power module subcomponents, which also depend on operating conditions and/or environment. The beginning of this phase can be considered as the power switch lifetime during the design process.

The military handbook reliability prediction of electronic equipment, MIL-HB-217F, predicts a mean time to failure (MTTF) of an IGBT module of 78 years, but this is only valid for discrete devices and not for modules containing multiple integrated components. Higher accuracy lifetime expectancy prediction methods considering also operating conditions must be considered. Two different approaches exist to predict power switch lifetime: physics of failure models, and empirical-based models. The first approach is based on the study of the intrinsic failure cause, like electrical stress, thermal stress, chemical composition, etc. On the other hand, empirical-based models use results coming from accelerated tests to provide an estimation of the failure rate at different operating conditions. Although many different types of accelerated tests are normally conducted by the manufacturer (humidity, vibration, low temperature storage, reverse bias, etc.), the main factor that can produce a failure in a power switch module is power cycling\(^8\).

Power switch manufacturers perform statistical approaches from a group of samples to estimate power module lifetime. This prediction is usually presented as a relationship between the number of temperature swings (or power cycles) and delta of temperature variation during swings. The number of cycles is assumed to be proportional to \(\Delta T_j^\alpha\) (being \(\Delta T_j\) the junction temperature swing; and \(\alpha\), a constant), as it appears as a straight line when plotting \(\log(N_f)\) over \(\log(\Delta T_j)\).

However, power cycling lifetime also depends on the absolute medium junction temperature (\(T_m=T_{j,min}+\Delta T_j/2\)), as shown on figure 98. An Arrhenius factor is thus added to the typical Coffin-Manson law (plastic deformation fatigue), as shown in (72). \(N_{CP}\) is the number of cycles to failure, \(k_B\) is the Boltzmann-constant. The constant \(A\), the exponent \(\beta\) and the activation energy \(E_a\), are parameters obtained by least-square-fit of experimental accelerated thermal stress tests to failure on expression (72).

---

\(^8\) Periodic temperature swing on power switch junction causing long-term physical damage.
A more detailed lifetime model taking into account the influence of other parameters like turn-on time, $t_{on}$, current per bond foot, $I_b$, voltage class, $V_c$, and bond wire diameter, $D$, is shown in (73). However, the influence of each $\beta$ parameter must be obtained using curve-fitting algorithms from experimental data.

$$N_{cf} = A \Delta T_j^{\gamma} \cdot e^{\frac{E_a}{k_B T_m}} \cdot e^{\frac{\beta_2}{T_j^{\beta_2}}} \cdot t_{on}^{\beta_3} \cdot I_b^{\beta_4} \cdot V_c^{\beta_5} \cdot D^{\beta_6}$$

(73)

In practice power switch lifetime is usually calculated using the power cycling lifetime curves provided by the manufacturer, as shown on figure 99 for Infineon IGBT4 modules from Infineon. Once the temperature rise in the power switch junction, $\Delta T_j$, is calculated using the thermal models presented in 5.2, the number of estimated cycles to failure, or power switch lifetime, can be read from this curve. However, as the power cycling test time can be different from the user cycle time for each application, this result must be scaled using the following expression:

$$N_{user} = N_{test} \cdot \left(\frac{t_{on(user)}}{t_{on(test)}}\right)^{\beta_3}$$

(74)
The special case of extended FBSOA MOSFETs, power cycling lifetime curves are not provided by the manufacturer, and FIT curves for power MOSFETs are usually not available. Manufacturers only perform 360000 cycles with a ∆T of 100 ºC on a given production sample size (approximately 25 units), which does only provide the indication that the MOSFETs can survive this amount of cycles and thermal cycling. In the absence of these curves, and as a conservative approach, the IGBT curves of Figure 99 will also be applied to the linear stage MOSFETs. Further studies are required to create an accurate MOSFET lifetime prediction model.

The analytical power switch lifetime models presented in this section 5.3 have been integrated in the lifetime design model of the Power Electronics System Design tool. The integration details are described in chapter 7.
5.4 Simplified inductance dimensioning model

The simplified dimensioning model for the inductances is based on curve fitting of the volumes and prices of the power inductances ordered by CERN during the last 10 years, as a function of the magnetic energy stored in the inductance $W_{mag}$.

\[ W_{mag}[J] = \frac{1}{2} L I^2 \]  

(75)

Figure 100 shows the inductance cost as a function of the magnetic energy stored. It is possible to approximate the inductance cost with a first order linear approximation, as shown in (76).

\[ Price_{ind}[\text{Eur}] = 21,398.W_{mag} + 358.91 \]  

(76)
The inductance volume as a function of the magnetic energy stored is shown on Figure 101, and the function can be approximated by (77). The inductance volume predicted by this expression has been further verified by using detailed analytical inductance design models described in Annex A.

\[ Volume_{ind}[m^3] = 0.0002 \cdot W_{mag} + 0.0018 \]  

(77)

![Figure 101 Inductance volume versus magnetic energy stored](image)

On this simplified inductor dimensioning model, the copper and magnetic losses in the inductor have been neglected. Its integration in the Power Electronics System Design tool is described in 7.1.1.1, and illustrated on figures 137 and 138. A fine inductor dimensioning model, with higher precision but heavier in terms of computing time required, has also been developed and it is presented in Annex A. This fine inductor dimensioning model has been applied to the inductor derived from the optimization problem of 7.1.1.1, that utilizes the simplified inductor dimensioning model, to verify that the magnetic losses in the inductance can be neglected with respect to the total losses in the power converters. A more detailed explanation of this validation to the specific optimal solutions obtained in chapter 7 are described in Annex A. The validation also shows that the inductance and core temperature constraints are always respected.
5.5 Capacitor dimensioning model

In the same way as performed for the inductance design model, the capacitors cost and volume of an important number of capacitors\(^9\) from different vendors ordered at CERN during the last 10 years as a function of energy stored, is plotted on figure 102. A tendency line based on a first order linear approximation can be calculated, as shown in (79).

\[
W_{\text{cap}} = \frac{C \cdot V^2}{2} \tag{78}
\]

\[
\text{Price}_{\text{cap}} [\text{Eur}] = 0.1354 \cdot W_{\text{cap}} + 54.119 \tag{79}
\]

Figure 102 Capacitor cost versus energy stored

\(^9\) The considered capacitors had voltage ratings ranging from 100V to 100kV
The evolution of the capacitor volume as a function of $W_{\text{cap}}$ is shown on Figure 103. Its tendency can be approximated by a first order linear approximation, resulting in the following expression:

$$V_{\text{cap}}[m^3] = 3 \times 10^{-6}. W_{\text{cap}} + 0.0027$$

(80)

![Figure 103 Capacitor volume vs energy stored](image)

The capacitor cost and volume design models have been integrated in the capacitor design model of the Power Electronics System Design tool, as illustrated on figures 137 and 138 of chapter 7.
5.6 Linear converter model for design purposes

The output current control of the active bouncer high current stage (HCS) is performed by using a hysteresis controller. This control method is selected because it maximizes the dynamic performances of the system providing a very fast response. This is critical for CLIC application, as the pulse length $t_{flat}$ is quite short.

The way the HCS current hysteretic controller operates, consists in applying the full capacitor bank voltage $V_{AB}$ (see figure 104) into the HCS output filter when the active bouncer current goes below a lower threshold $I_{B_{min}}$ and removing this voltage when the current exceeds a upper threshold $I_{B_{max}}$. This concept is illustrated on figure 105.

![Figure 104 High current stage with Modulator pulse transformer equivalent circuit](image-url)
Due to the fact that the active bouncer produces a voltage ramp, the current slew rate during the pulse changes according to the following expression:

\[
\frac{di}{dt} = \frac{V_{AB} - V_{bouncer}}{L_b}
\]  

(81)

As the hysteresis thresholds are constant, the switching frequency changes during the pulse. The maximum and minimum switching frequencies are achieved at the beginning and at the end of the pulse, being respectively:

\[
f_{\text{max}} = \frac{V_{AB}}{L \Delta i}
\]

(82)

\[
f_{\text{min}} = \frac{V_{AB} - V_{bouncer \text{,max}}}{L \Delta i}
\]

(83)
With a maximum level of ripple content at the klystron $V_{\text{sec}}$ specified for 100 ppm for example, it is possible to verify if a given design and hysteresis band respects this specification. This can be performed by calculating the attenuation provided by the HCS load at $f_{\text{max}}$ and $f_{\text{min}}$. This amplitude of the output switching harmonics at the klystron can be computed with the following expression:

$$\Delta V_{\text{sec}} = \left| \frac{V_{\text{sec}}(s)}{V_{b}(s)} \right|_{f_s} \cdot V_{AB} \cdot tr$$  \hspace{1cm} (84)

Where $\left| \frac{V_{\text{sec}}(s)}{V_{b}(s)} \right|_{f_s}$ is the modulus or gain value of the transfer function between the klystron voltage $V_{\text{sec}}$ and the voltage supplied by the HCS $V_{b}$, at the switching frequency $f_s$. $tr$ is the step-up pulse transformer turns ratio.

The analytical models presented in this section 5.7, have been integrated in the control design models of the Power Electronics System Design tool, as it will be further explained in chapter 7.
CHAPTER VI

6  EXPERIMENTAL VALIDATION

Reduced scale prototypes have been constructed to experimentally validate the correct operation of the selected topology Split Power And Droop Compensator (SPDC), previously presented in 3.4. The Fast Voltage Compensator (FVC) and the Active Bouncer prototype test results will be presented hereafter. Two factors have been considered to select the primary voltage of the modulator prototype:

- The primary voltage value had to be adapted to perform the feasibility study of reduced-scale transformer prototypes.
- The voltage range had to be adapted to validate models and intended technology for CLIC

As a result, a primary voltage of 1 kV, which allows to test 600 V, 1.2 kV and 1.7 kV IGBT technologies, was selected.

6.1 Fast Voltage Compensator - FVC

With the purpose of experimentally validating the operation principle of the proposed FVC and compare its performance versus the same system without FVC under different capacitor charger control strategies, a reduced scale modulator prototype has been designed and constructed. Figure 106 shows the prototype topology and Table 9 presents the main circuit parameters values. The selection of component values was influenced by the availability of off-the-shelf components, in order to advance with the construction as soon as possible.
In all the experimental tests, the modulator main capacitor bank $C_{\text{main}}$ was charged to 537 V and discharged into a RL load, to simulate the klystron equivalent resistance and the leakage inductance of the pulse transformer, respectively. With these conditions, the capacitor bank experiences a transient process.

Figure 107 shows an image of the constructed modulator equipped with the FVC prototype, and a closer view to the three FVC IGBT H-bridges. In all the experimental tests, the modulator main capacitor bank $C_{\text{main}}$ was charged to 537 V and discharged into a RL load, to simulate the klystron equivalent resistance and the leakage inductance of the pulse transformer, respectively. With these conditions, the capacitor bank experiences a transient process.

### Table 9 Reduced-scale modulator prototype parameters

<table>
<thead>
<tr>
<th>Capacitor charger</th>
<th>1200 V, 3500W</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{main}}$</td>
<td>960 $\mu$F (film)</td>
</tr>
<tr>
<td>$L_k$</td>
<td>64 $\mu$H</td>
</tr>
<tr>
<td>$R_{\text{load}}$</td>
<td>9.4 $\Omega$</td>
</tr>
<tr>
<td>$R_{\text{demag}}$</td>
<td>1 $\Omega$</td>
</tr>
<tr>
<td>$L_{\text{FVC}}$</td>
<td>350 $\mu$H</td>
</tr>
<tr>
<td>$C_{\text{FVC}}$</td>
<td>22 $\mu$F (film)</td>
</tr>
<tr>
<td>$C_{\text{Bank}}$</td>
<td>22600 $\mu$F (electrolytic) + 2400 $\mu$F (film)</td>
</tr>
<tr>
<td>$T_{1a},D_{1a},T_{1b},D_{1b},T_{1c},D_{1c},T_{1d},D_{1d}$</td>
<td>2 x IGBT half-bridge 600V 70A modules</td>
</tr>
<tr>
<td>$D_{\text{main}},T_{\text{main}},D_{\text{demag}}$</td>
<td>1 x IGBT 1700V 450A module</td>
</tr>
<tr>
<td>Pulse Width</td>
<td>1 ms</td>
</tr>
<tr>
<td>Repetition Rate</td>
<td>1 Hz</td>
</tr>
</tbody>
</table>
a discharge of 56 V during each 1 ms long pulse. A demagnetization circuit branch composed by a diode and a 1 Ω resistance was used to dissipate the energy stored in the transformer leakage inductance $L_k$ at the end of each pulse.

Experimental results of power fluctuation levels respectively obtained with the modulator without FVC and equipped with a FVC for different capacitor charger operating modes are presented in the following subsections.

Figure 107 Reduced scale modulator prototype (left) and detailed view of the three FVC H-bridges (right).
6.1.1 Modulator operation without FVC

6.1.1.1 Capacitor charger operated in voltage control mode

In this first test, the capacitor charger was operated under voltage control mode while the modulator pulses on a resistive load with a repetition rate of 1 Hz. Figure 108 shows the charger operation during the pulse and Figure 109 shows the main waveforms during two cycles, where \( P \) stands for the capacitor charger instantaneous power on the DC side \((P = V_{ch} \times I_{ch})\). One can observe how, after a small delay, the charger tries to correct the voltage drop produced during the pulse. As a consequence, capacitor charger instantaneous output power suddenly rises to 2350 W, even though this consumption only lasts some milliseconds before dropping to almost zero. If we consider that the average consumption of the modulator in this specific example and operation mode is 27.28 W, the equivalent power fluctuation defined by (85) would be in this case 8614 %. Please notice that this value is higher than 100 % due to the fact that the power fluctuation is defined with respect to the average power consumption.

\[
\Delta P(\%) = \left( \frac{P_{\text{max}} - P_{\text{min}}}{P_{\text{average}}} \right) \cdot 100 \tag{85}
\]
Figure 108 Modulator waveforms during the pulse (charger operated in voltage mode control)
6.1.1.2 Capacitor charger operated in constant current control mode

In this second test, the capacitor charger was operated under constant current control mode. The current reference was configured to match the corresponding average charging current for this experimental set-up and specific operation mode, with the purpose of obtaining a repeatable capacitor voltage value at the beginning of each pulse. Figure 110 shows the charger operation during the pulse and Figure 111 shows the main waveforms during several cycles. We observe that the capacitor charger successfully maintains the charging current almost constant. It only experiences a small variation during the pulse, due to the charger current regulation bandwidth limitations. In this case the peak power achieved is only 29.3W, and the power fluctuation is 12.97%. However one has to notice that the power consumption is never constant. This case corresponds to the one previously illustrated on figure 35.B).
Figure 110 Modulator waveforms during the pulse, charger under constant current control
6.1.2 Modulator operation with FVC

In this third and last test, the modulator prototype is equipped with the proposed FVC. Due to the fact that during the pulse the capacitor bank experiences a voltage drop of 56 V and the FVC consists in a 4-quadrant H-bridge topology, the voltage operating range of the FVC has been set from -28 V to +28 V. The FVC DC bus was charged to 100 V. A simple hysteretic voltage regulator was used to control the FVC, instead of a double RST controller structure, in order to avoid the complexity of implementing these algorithms on FPGA/DSP. The control is performed using a custom designed electronic card based on a FPGA and equipped with 3 mega-samples per second analog to digital converters. The hysteresis thresholds were set to -0.5 V and +0.5 V respectively. Figures 112 and 113 show the modulator and FVC waveforms during the pulse and during several
cycles, respectively. It can be seen how the peak power level achieved is only 27.9W and that the power fluctuation has been successfully reduced to 1.76%.

Figure 112 Waveforms of the modulator equipped with FVC prototype during the pulse (charger under constant current control)
Figure 113 Waveforms of the modulator equipped with FVC prototype during several cycles (charger under constant current control)

It is important to notice that, in this specific test, the average charging current is very low and, therefore, the charging current ripple and the FVC voltage ripple highly contribute to increase the power fluctuation levels. Much lower power fluctuation values can be expected from a higher average power modulator. However one can see how the instantaneous power is constant during the whole operation of the modulator presenting a small
fluctuation. However, the frequency of this fluctuation is in the order of 20 kHz, meaning that it can be easily filtered by a dedicated small passive filter.

As a conclusion to the experimental tests, we can state that the proposed FVC, rated only at a fraction of the charging voltage and capable of handling the charging current, appears to be an appropriate solution to achieve constant power consumption from the performances optimization point of view (e.g. efficiency and cost). It has been experimentally demonstrated that it is capable of correctly stabilize the charging power when implemented in conjunction with a commercial capacitor charger based pulsed power converter.

### 6.2 Active Bouncer

#### 6.2.1 Experimental Validation

With the purpose of validating the operation of the proposed Active Bouncer topology, a reduced scale prototype has been constructed, following the schematic depicted in Figure 114. We can see that a saturable inductance $L_{sat}$ has been placed in series with the recovery diode $D_f$, in order to slow down the current slope when $D_f$ becomes forward-biased after each pulse. The linear stage is composed of four linear MOSFETs from Ixys, $M_1$, $M_2$, $M_3$, and $M_4$; and a shunt resistor $R_{shunt}$ is used to measure the current provided by the linear stage. Table 10 shows the values chosen for each passive component, and Table 11 details the power electronic components chosen for the prototype.

![Figure 114: Active Bouncer prototype with LS and HCS schematic](image-url)
Table 10 Active Bouncer prototype passive component values

<table>
<thead>
<tr>
<th>Component</th>
<th>Symbol</th>
<th>Value</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCS inductances</td>
<td>$L_1$, $L_2$, $L_3$</td>
<td>303 µH</td>
<td>Custom made</td>
</tr>
<tr>
<td>Simulated transformer leakage inductance</td>
<td>$L_K$</td>
<td>66 µH</td>
<td>Custom made</td>
</tr>
<tr>
<td>Recovery saturable reactor</td>
<td>$L_{sat}$</td>
<td>2 µH</td>
<td>Custom made</td>
</tr>
<tr>
<td>Main capacitor bank</td>
<td>$C_{main}$</td>
<td>960 µF</td>
<td>2 x 480 µF EPCOS Film</td>
</tr>
<tr>
<td>Active Bouncer capacitor bank</td>
<td>$C_{AB}$</td>
<td>26.4 mF</td>
<td>400 V DC Semikron Film</td>
</tr>
<tr>
<td>Active Bouncer output filter capacitor</td>
<td>$C_o$</td>
<td>2.5 µF</td>
<td>EPCOS snubber capacitor</td>
</tr>
<tr>
<td>Active Bouncer damping capacitor</td>
<td>$C_{df}$</td>
<td>12 µF</td>
<td>4 x EPCOS snubber capacitor</td>
</tr>
<tr>
<td>Active Bouncer damping resistor</td>
<td>$R_{df}$</td>
<td>0.25 Ω</td>
<td>4 x Parallel 1 Ω Vishay Film</td>
</tr>
<tr>
<td>Active Bouncer filter discharging resistor</td>
<td>$R_f$</td>
<td>50 Ω</td>
<td>2 x 100 Ω Arcol HS300</td>
</tr>
<tr>
<td>Demagnetization resistor</td>
<td>$R_d$</td>
<td>1 Ω</td>
<td>Arcol HS300</td>
</tr>
<tr>
<td>Simulated klystron resistor</td>
<td>$R_{kly}$</td>
<td>9.4 Ω</td>
<td>5 x Parallel 47 Ω Arcol HS300</td>
</tr>
<tr>
<td>LS shunt resistor</td>
<td>$R_{shunt}$</td>
<td>2.5 m Ω</td>
<td>Murata 20A 50mV 0.25%</td>
</tr>
</tbody>
</table>

Table 11 Active Bouncer power electronics components

<table>
<thead>
<tr>
<th>Component</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEMIX653GAR176H Ds</td>
<td>$S_{SC}$, $S_R$, $S_t$, $D_1$</td>
<td>1700V, 450A, IGBT+Diode GAR Trench IGBT module</td>
</tr>
<tr>
<td>Skyper 32 PRO R</td>
<td>$S_{SC}$, $S_R$, $S_t$</td>
<td>15A peak Semikron IGBT Driver</td>
</tr>
<tr>
<td>SKM 195GB066D</td>
<td>$T_1$, $T_2$, $T_3$, $D_1$, $D_2$, $D_3$</td>
<td>600V, 200A, Half-bridge Trench IGBT module</td>
</tr>
<tr>
<td>SKHI 23/12</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>8A peak Semikron Half-bridge IGBT Driver</td>
</tr>
<tr>
<td>SKKE 162/16</td>
<td>$D_K$</td>
<td>1600V, 174A Semikron SemiPack 2 Diode Module</td>
</tr>
<tr>
<td>UFB200FA40P</td>
<td>$D_f$</td>
<td>400V, 200A Ultrafast Vishay Dual Rectifier Module</td>
</tr>
<tr>
<td>IXTH30N50L2</td>
<td>$M_1$, $M_2$, $M_3$, $M_4$</td>
<td>500V, 30A, Ixys Extended FBSoA LinearL2 Power Mosfet</td>
</tr>
</tbody>
</table>

The linear stage MOSFETs, were driven by a high current buffer BUF634, capable of providing 250mA with a configurable bandwidth between 30 MHz and 180 MHz, as shown on Figure 115.
The linear stage was controlled in current with a control loop directly implemented in analog, in the form of an error amplifier, as shown on figure 116. The current was measured using the current shunt $R_{\text{shunt}}$.

Figure 116 Linear stage current control with Error Amplifier

The bandwidth of the linear stage was verified by applying as reference a double step, and fitting the response as a 2\textsuperscript{nd} order polynomial. System response is depicted on figure 117, and corresponds to the following values:

- Bandwidth: \(~3\) MHz
- Damping: 0.83
- Transport delay: 56 ns
The full prototype assembly is shown on Figure 118. Figures 119 and 120 provide a closer view of the Linear Stage and High Current Stage prototypes, respectively.
Figure 118 Reduced Scale Modulator prototype equipped with proposed Active Bouncer topology.
Figure 119 Linear Stage (LS) power converter

Figure 120 High Current Stage (HCS) power stack
The tests have been performed considering a pulse width of 1 ms. The main capacitor bank was initially charged to 450 V, while the active bouncer DC bus was charged to 150 V. The three HCS phases have been controlled using a common control signal coming from a hysteresis current controller with error bands of ±2.5 A. The LS featured a current control loop implemented directly with analogue components. The current reference for the LS was generated using an external waveform generator (open loop operation).

Figure 121 shows the measurements of the output voltage pulse $V_p$, the primary current $I_p$, the modulator capacitor voltage $V_{CAP}$, and the active bouncer output voltage $V_{bouncer}$. We observe how the main capacitor bank experiences a progressive discharge of 55 V during the pulse, which is compensated by the corresponding progressive increase of the active bouncer output filter capacitor voltage $V_{bouncer}$. At the end of the pulse, when the main switch $S_1$ opens, we can notice how $V_{bouncer}$ increases very fast, due to the fact that the energy stored in the HCS inductances is transferred to $C_b$. When $V_{bouncer}$ achieves the same voltage level as the Active Bouncer DC bus voltage $V_{AB}$, the diode $D_f$ is forward-biased and starts conducting to recover the energy back to $C_{AB}$.

Figure 122 shows a zoom on the output voltage pulse. We observe the presence of the active bouncer switching harmonics, which remain contained within a maximum error band amplitude of 1 V peak to peak. This means that the corresponding voltage stability achieved is:

$$E_{\text{prototype}} \% = \frac{(V_{P, \text{max}}-V_{P, \text{min}})_{\text{pulse}}}{V_{P, \text{nom}}} \times 100 = \frac{1}{450} \times 100 = 0.22 \%$$  \hspace{1cm} (86)
Figure 121 Output voltage pulse, primary current, main capacitor voltage and Active Bouncer filter output voltage produced by the modulator prototype equipped with the SPDC topology
Figure 122 Zoom on the output voltage pulse produced by the modulator prototype equipped with the SPDC topology

Even if the achieved voltage stability remains well below the 1% voltage stability specification required for the CLIC modulator, we also have to consider that the ratio between the nominal primary voltage and the voltage excursion compensated during the experimental validation by the active bouncer is much higher than in the full-scale CLIC klystron modulator:

\[
V_{\text{ratio\_prototype}} = \frac{55 \, \text{V}}{450 \, \text{V}} = 0.1222
\]  
(87)

\[
V_{\text{ratio\_modulator}} = \frac{800 \, \text{V}}{20000 \, \text{V}} = 0.04
\]  
(88)

This means that, considering a value of 20 kV for the primary voltage of the full scale prototype, the compensating ratio in the prototype is three times higher than the one required in the full scale modulator. Due to the fact that the primary voltage is the sum of the modulator capacitor bank voltage \( V_{\text{CAP}} \) and the active bouncer output filter capacitor voltage \( V_{\text{bouncer}} \), the full-scale modulator output voltage stability using a similar active bouncer power converter would be:

\[
E_{\text{modulator}} \% = \frac{1 \, \text{V}}{20000 \, \text{V}} \times 100 = 0.005 \%
\]  
(89)
This stability value would correspond to 50 ppm. However one has to take into account that the prototype HCS filter inductances value could be increased much further (especially considering the parallel and simultaneous operation, instead of interleaving, of the three phases during the experimental test, that reduced the equivalent inductance to just one third) to obtain a higher attenuation of the switching harmonics. Multiphase interleaving would also help in reducing the amplitude of the switching harmonics. The linear stage LS could also help to achieve better stability values by implementing a feedback loop, or a pulse to pulse learning algorithm, such that it provides compensation for the harmonics generated by the HCS.

Figure 123 shows, in addition to the output voltage pulse $V_p$ and the Active Bouncer output filter voltage $V_{\text{bouncer}}$, the evolution of the Active Bouncer capacitor bank voltage $V_{\text{AB}}$, the current provided by the HCS $I_{\text{HCS}}$, the current provided by the LS $I_{\text{LS}}$, and the gate-source voltage applied to the linear MOSFETs $V_{\text{GATE}}$. Due to the high value of the Active Bouncer capacitor bank, it just experiences a very little discharge. We also observe how the HCS current drops with time, and how the linear stage provides a current ramp starting at 0 A when the nominal flat-top voltage is achieved. It is important to notice that a voltage offset has been applied to the MOSFET gate-source voltage (just below its threshold voltage $V_{\text{GS(th)}}$) to make faster the transition to linear mode from the blocking state. Due to the low capacitance value of the output filter, the LS only has to provide a peak current value of 2 A, thus minimizing the LS power requirements and maximizing the efficiency of the whole system.
Figure 123 $V_P$, $V_{AB}$, $V_{bouncer}$, $I_{HCS}$, $I_{LS}$, and $V_{GATE}$ waveforms during a pulse
On figure 124 we can observe respectively how:

- The voltage pulse $V_p$ builds up together with its control signal $S_1$.
- The HCS control signals $T_1$, $T_2$, $T_3$ control and generate the voltage harmonics on $V_{bouncer}$.
- The current in the short-circuit switch $I_{SC}$ rises before the pulse together with its control signal $S_{SC}$.

Figure 124 $S_1$, $V_p$, $T_1$, $T_2$, $T_3$, $V_{bouncer}$, $S_{SC}$, and $I_{SC}$ waveforms during a pulse.
One can notice on figure 125 shows how the active bouncer output filter voltage $V_{bouncer}$ is discharged to the zero voltage initial condition before the start of a new pulse. The discharge is performed by closing the switch $S_R$, which connects the filter to the resistor $R_R$ with a value of 50 $\Omega$. The maximum current in the $S_R$ switch, $I_{SR}$, does not exceed 3.1 A and lasts about 2 ms. It is important to notice that, due to the reduced value of $C_b$, an extremely low current is enough to charge it to a certain voltage between two pulses (1 sec).

![Graph](image)

**Figure 125** $V_p$, $V_{bouncer}$, $S_R$, and $I_{SR}$ before and after a modulator prototype pulse

Figure 126 shows the current and voltage waveforms in the demagnetization branch. At the end of the output voltage pulse $V_P$, the diode $D_1$ starts conducting and the current $I_{demag}$ rises up to a maximum of 33 A. The voltage across the resistor $R_d$ rises accordingly to 33 V, as the resistor value is 1 $\Omega$. 

151
Figure 127 shows the energy recovery process after a pulse. When $S_1$ opens, the voltage in the active bouncer output filter $V_{\text{bouncer}}$ increases to 150 V, the current in the HCS phases starts decreasing as the energy stored in the $L_1$, $L_2$ and $L_3$ inductances transfer their stored energy into $C_0$. Once $V_{\text{bouncer}}$ achieves 150 V the diode $D_f$ starts conducting. The current transferred back to the active bouncer capacitor bank $I_{\text{Rec}}$ has a peak value of 30 A, which represents an energy recovery of 0.09 J. Even if this value could seem low, one has to take into account that in the full scale modulator the current value in the HCS phases will not be just 50 A. In this case, it will reach values greater than 2000 A, the DC bus will not be 150 V, but 800 V, and the output filter inductance value will be also much higher. All these factors imply a much higher recovered energy in the full-scale prototype.
Figure 127 \( V_{bouncer}, I_{HCS}, \) and \( I_{Rec} \) after a modulator prototype pulse

Figure 128 shows the parallel connected Arcol HS300 resistors used as restive load to emulate the klystron load. Figure 129 shows the IGBT reset assembly composed of a Semikron IGBT in series with 2 parallel connected Arcol HS300 resistors. Figure 130 shows the fast recovery diode \( D_f \) assembly. The inductor that is emulating the transformer leakage inductance is presented in figure 131. This inductor was constructed using two "C" shape laminated silicon iron yokes with a 2 mm air gap. The coil conductor used for this application was a Litz wire cable with nylon isolation composed of 630 isolated copper wires with a diameter of 0.2 mm. This conductor was also used to construct the active bouncer HCS output filter inductances.
Figure 128 Modulator load $R_{mod}$ made of several parallel connected Arcol HS300 resistors.

Figure 129 Reset IGBT switch $S_R$ and two parallel connected resistors $R_R$
Figure 130 Recovery diode $D_f$ mounted on a heat sink together with a spare diode.

Figure 131 Custom made inductance $L_k$ used to simulate the transformer windings leakage inductance.
Figure 132 shows a picture of the oscilloscope during the measurements. We can see a zoom on the output voltage pulse $V_P$; the current provided by the linear stage $I_{LS}$; the primary current; and the active bouncer output filter voltage $V_{bouncer}$.

![Oscilloscope with waveforms](image)

Figure 132 Oscilloscope with the following waveforms: $V_P$ in yellow; $I_{LS}$ in blue; $I_P$ in purple; and $V_{bouncer}$ in green
6.2.2 Comparison with numerical simulation results

With the purpose of evaluating the precision of the numerical simulation model with the experimental results, a numerical simulation using SimPowerSystems was carried out. In this simulation the IGBTs have been modelled like ideal switches and the active bouncer phases as ideal voltage sources producing square pulses from 0 V to 150 V. The linear stage LS has been modelled as an ideal current source. Please notice that propagation delays introduced by the driver, together with the ADC acquisition time, have also been considered and modelled as a 3 µs transport delay in the active bouncer HCS phases. The values of the different passive components are the same as the ones used in the prototype that are listed on Table 11. The SimpowerSystems Matlab Simulink simulation model is depicted on figure 133.

![Figure 133 SimpowerSystems Matlab Simulink Simulation model of the reduced-scale modulator prototype equipped with the SPDC topology](image)

Figure 134 respectively shows the simulated waveforms of the output voltage pulse $V_P$, the voltage on the main capacitor bank $V_{CAP}$, the active bouncer output filter voltage $V_{bouncer}$, the current provided by the High Current Stage and the current provided by the Linear Stage.
LS. We observe the same voltage excursion in the discharge of $V_{CAP}$ and the voltage ramp on $V_{bouncer}$. The current provided by the HCS also matches the one obtained in the experimental validation. The output voltage pulse $V_P$ however, is slightly different than the one measured in the prototype. The amplitude of the obtained voltage ripples are the same in the two cases, slightly less than 1 V. However, in the simulation one can observe an oscillation during the settling time that causes the voltage stability of the pulse to be 2 V instead of the 1 V obtained in the experimental validation. Two possible reasons can explain this difference. The first one is the opening of $S_{SC}$, which occurs instantaneously in the simulation model and creates a small instability. The second one is the reference value provided to the linear stage, which in the case of the signal generator could be slightly different than the one applied in simulation. The start of the LS current reference was optimized during several experimental trials by modifying it with the signal generator waveform settings, while in the simulation the current was set to start ramping as soon as the output voltage pulse $V_P$ starts to rise. The same LS start reference strategy could also be modelled in simulation in order to match the same ripple amplitude as in the experimental validation, but this difference has been intentionally kept in order to show the differences between the results using the same design models used for dimensioning, and the ones obtained experimentally.
Figure 134 Simulated waveforms of the modulator prototype equipped with SPDC during a pulse: Zoom on the output voltage pulse $V_P$; voltage on the main capacitor bank $V_{CAP}$; active bouncer output filter voltage $V_{bouncer}$; $I_{HCS}$; and $I_{LS}$.

As a conclusion to this chapter, the proposed and retained SPDC topology presented in chapter 3.2 to perform power and droop compensation, has been successfully experimentally validated. Following the methodology depicted on Figure 68 in chapter IV, the design models presented in chapter V will now be integrated into a global optimal dimensioning tool in chapter VII. This dimensioning tool will be used to optimally dimension a full-scale modulator respecting CLIC specifications.
CHAPTER VII

7 OPTIMAL DIMENSIONNING OF THE FULL-SCALE CLIC KLYSTRON MODULATOR

The optimal dimensioning of the CLIC klystron modulator is performed using the proposed constrained nonlinear optimization environment described in 4.2 and presented in [110], which is based on space mapping techniques [111][112][113]. This approach makes possible to achieve a more efficient optimization process by using two dimensioning models with different levels of accuracy and complexity: a coarse model with lower accuracy but with faster computation time (in this specific application, the power electronics system design tool using the analytical and frequency-domain design models presented in chapter V), and a fine model with improved accuracy but requiring much longer computation times (in this specific application, a numerical simulation model). The coarse model is used for a numerical optimization process, while the fine model is used to validate the intermediate optimal solutions. If differences between the results obtained by the two dimensioning models are found, correction factors are introduced to improve the precision of the coarse models from the numerical simulation results. A new iteration of this process is launched again until convergence between the results obtained with the two dimensioning models is achieved. This method allows using the numerical simulation in an efficient way, where typically less than ten correction iterations are required to achieve convergence between analytical models and numerical simulation, as shown in [110]. The particular application of this method to the active bouncer and fast voltage compensator design introduces the additional complexity of dealing with discrete variables, as the number of phases of these converters has to be an integer number. To cope with this issue, the optimal modulator design is split in three different optimization phases, as shown on figure 135.
In the first phase, design optimization sweeps are performed for different voltage droop values corresponding to different $C_{\text{main}}$ sizes. Due to the nature of the nonlinear optimization algorithms, the number of phases is treated as a continuous variable. As a result of these first optimization sweeps, the optimal voltage droop and IGBT switch technology is identified.

The second phase explores the optimal voltage droop value and switch technology identified during the first phase, by performing optimization sweeps for different number of phases (discrete variable). The outcome of this second phase is the identification of the optimal number of phases and IGBT switch.

The third and final phase consists in the validation and correction of the analytical design models via numerical simulation. Several iterations are performed until reaching convergence between simulation and analytical results, leading to the final optimal design results.

Two design input parameters will be considered for the optimal dimensioning of the klystron modulator for CLIC. The first one is the primary modulator primary voltage. The research collaboration with Nottingham University on CLIC [114][115][116], demonstrated that the great economical advantage of selecting 20 kV as primary voltage. Additional studies performed at Laval University, also demonstrated that increasing the primary voltage to this value, would also reduce the size and cost of the active bouncer and pulse transformer. Consequently, a modulator primary voltage value of 20 kV will be imposed. The second optimization input parameter is the pulse transformer, also designed and subject of a different PhD dissertation at Laval University [117][118][119][120][121]. The parameters of the calculated pulse transformer equivalent circuit, referred to the primary side and depicted on figure 136, are presented in table 12.
Table 12 Pulse transformer equivalent circuit parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance: $L_m$</td>
<td>28 mH</td>
</tr>
<tr>
<td>Leakage inductance: $L_k$</td>
<td>20.3 µH</td>
</tr>
<tr>
<td>Primary capacitance: $C'_{11}$</td>
<td>4.6 nF</td>
</tr>
<tr>
<td>Secondary capacitance: $C'_{22}$</td>
<td>58.1 nF</td>
</tr>
<tr>
<td>Primary winding resistance: $R_1$</td>
<td>15.6 mΩ</td>
</tr>
<tr>
<td>Secondary winding resistance: $R'_2$</td>
<td>17.7 mΩ</td>
</tr>
</tbody>
</table>

The optimization of the SPDC Active bouncer (HCS and LS) will be presented in 7.1, while the SPDC FVC will be presented in 7.2.

**7.1 SPDC Active Bouncer**

**7.1.1 Optimization Phase 1: optimal voltage droop and switch technology**

**7.1.1.1 Optimization problem formulation**

The nonlinear optimization algorithm, core of the proposed nonlinear optimization environment, minimizes the value of an objective function (in the specific application presented in this chapter: volume, price, losses or the weighted sum of the three of them) $f(x)$, such that:

$$A \cdot x \leq b$$

$$A_{eq} \cdot x = b_{eq}$$
\[ l_b \leq x \leq u_b \]  
\[ c(x) \leq 0 \]  
\[ c_{eq}(x) = 0 \]  

Where \( x, b, b_{eq}, l_b \) and \( u_b \) are the vectors of the design variables (specified in table 13), linear inequality constraints values, linear equality constraints values, variables lower bounds and variables upper bounds, respectively. \( A \) and \( A_{eq} \) are the matrixes containing the linear inequality equations and linear equality constraints values. On the other hand, \( c(x) \) and \( c_{eq}(x) \) are the nonlinear inequality constraints and nonlinear equality constraints, respectively.

### Table 13 Modulator and SPDC Active Bouncer Design Optimization Variables

<table>
<thead>
<tr>
<th>Design Variables</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_b )</td>
<td>Active bouncer inductance value (per phase)</td>
</tr>
<tr>
<td>( N_{phases} )</td>
<td>Number of phases</td>
</tr>
<tr>
<td>( C_d )</td>
<td>Capacitance on filter damping branch</td>
</tr>
<tr>
<td>( R_d )</td>
<td>Damping resistor on filter damping branch</td>
</tr>
<tr>
<td>( C_b )</td>
<td>Active bouncer output filter capacitor</td>
</tr>
<tr>
<td>( F_{sw} )</td>
<td>Switching frequency of High Current Stage</td>
</tr>
<tr>
<td>( HS_length )</td>
<td>Heat sink length</td>
</tr>
<tr>
<td>( HS_width )</td>
<td>Heat sink width</td>
</tr>
<tr>
<td>( HS_thickness)</td>
<td>Heat sink thickness</td>
</tr>
<tr>
<td>( HS_dtt )</td>
<td>Heat sink distance between fins</td>
</tr>
<tr>
<td>( HS_fh )</td>
<td>Heat sink fin height</td>
</tr>
</tbody>
</table>

In the optimal dimensioning of the klystron modulator for CLIC, \( A, b, A_{eq}, b_{eq} \) and \( c_{eq} \) are null. Only lower and upper bounds are imposed for the design variables, and maximum values are specified for nonlinear constraints, which actually are the following CLIC design specifications:

- Ripple amplitude on klystron anode-cathode voltage must not exceed 100 ppm.
- Minimum semiconductors lifetime of 20 years of operation.
- Junction temperature on semiconductors must not exceed 125 °C.
- Modulator pulse forming system efficiency must be higher than 98 %
• Active bouncer open loop bandwidth (at -3dB) must be higher than 7.1 kHz (frequency corresponding to CLIC pulse flat-top with, 1/t_{th}).\textsuperscript{10}

• Heat-sink surface must be bigger than the IGBTs baseplate surface.

Figure 137 shows a detailed description of the design models used to compute the objective function value. On this figure, each block or design tool has been developed based on the design models previously presented in chapter V. Orange color stands for imposed optimization input values, red indicates optimization variable, blue stands for intermediate calculated parameters, and green indicates output parameter measuring objective function related performances.

Figure 137 Objective function evaluation

\textsuperscript{10} A lower active bouncer bandwidth would exceed the compensation capability of the Linear Stage
Image 138 shows instead the description of the design models used to evaluate the nonlinear inequality constraints. Orange color again stands for imposed input values, red indicates optimization variables, blue stands for intermediate calculated parameters, and green indicates parameter measuring nonlinear inequality constraints values.
Figure 138 Nonlinear inequality contraints evaluation
7.1.1.2 Sensitivity analysis

Before presenting and evaluating the results of the sensitivity analysis performed on the different design models, it is important to understand that the modulator capacitor bank \( C_{\text{main}} \) is the parameter presenting more influence on modulator size, cost and performances. Its contribution appears on all optimization results graphs in this first optimization phase. Figure 139 shows how the energy stored in \( C_{\text{main}} \) decreases exponentially as a function of the voltage droop. On the other hand, figure 140 shows that the energy stored in the active bouncer capacitor bank, instead increases as a function of the voltage drop, due to the increase of voltage range (and energy), that this power converter must compensate. However, the energy stored in the active bouncer is several orders of magnitude smaller than the energy stored in \( C_{\text{main}} \). This means that it is more convenient, from the overall modulator size point of view, to tolerate a higher voltage droop of the main capacitor bank, and correct it with the active bouncer. The optimizations performed hereafter will clarify this point and evaluate the impact on other modulator performance parameters like total cost and efficiency.

In order to evaluate the sensitivity of the design models to each performance parameter used in the evaluation of the final objective function, several optimizations sweeps for voltage droops of \( C_{\text{main}} \) between 200 V and 1000 V in steps of 50 V, were performed. The three performed optimization sweeps have as individual objective functions volume, price and efficiency, respectively.

Figures 141, 142 and 143 show the evolution of the total volume of the modulator (excluding the pulse transformer and the main switch, whose volume remain constant as they are taking as constant design variables) as a function of the voltage droop using different IGBT switches, for the three different objective functions, respectively. We observe that the total volume decreases exponentially with the voltage droop. Only in the case of having as individual objective function the efficiency (losses minimization), the volume starts increasing again for voltage droops of more than 800 V.
Figure 139 Energy stored and size of $C_{\text{main}}$ as a function of its voltage droop during the pulse

Figure 140 Energy stored in $C_{\text{main}}$ and Active Bouncer as a function of its voltage droop during the pulse
Figure 141 Total Volume - Volume optimization

Figure 142 Total volume - Price optimization
Figures 144, 145 and 146 show the evolution of the PFS efficiency for each of the three objective functions. One can notice that the PFS efficiency always decreases in a linear way for increasing values of voltage droop in the main capacitor bank. This makes sense as for compensating higher voltage droops, the active bouncer has to provide higher average power, and therefore presents higher loses. This tendency has a direct impact in the 20 years operation cost results that will be presented later on.
Figure 144 PFS efficiency - Volume optimization

Figure 145 PFS efficiency - Price optimization
Figure 146 PFS efficiency - Efficiency optimization
Figures 147, 148 and 149 show the evolution of the total cost of the modulator components, for each of the three objective functions. These graphs show the same tendency as the one obtained during the total modulator volume optimization, decreasing exponentially with the voltage droop, and only increasing again in the case of optimizing the efficiency alone for voltage droop values higher than 800 V. The meaning of this result is that maximizing all IGBT operating range must be exploited to find an optimal solution in terms of price.

Figure 147 Total cost - Volume Optimization
Figure 148 Total cost - Price optimization

Figure 149 Total cost - Efficiency optimization
Figures 150, 151 and 152 show the evolution of the operational cost of the modulator during 20 years of operation as a function of the voltage droop, for each of the three objective functions. This cost value corresponds only to the cost increase due to electrical losses in the system. We observe than in all cases, the operating cost increases linearly with voltage droop. This means that the modulator initial cost and operating cost evolve in an opposite way as a function of the voltage droop.

Figure 150 Operating cost for 20 years - Volume Optimization
Figure 151 Operating cost for 20 years - Price optimization

Figure 152 Operating cost 20 years operation - Efficiency optimization
Figures 153, 154 and 155 show the evolution active bouncer switching frequency as a function of the voltage droop, for each of the three objective functions. From the graphs tendency, the optimal switching frequency for 1700V IGBT switch technology seems to be between 20 kHz and 30 kHz; while for 1200V IGBT switch technology the optimal switching frequency would be slightly higher, between 30 kHz and 40 kHz.

Figure 153 Optimum switching frequency - Volume optimization
Figure 154 Optimum switching frequency - Price optimization

Figure 155 Optimum switching frequency - Efficiency optimization
Figures 156, 157 and 158 show the evolution of the number of phases as a function of the voltage droop, for each of the three objective functions. These results are directly related to the previously presented switching frequency values. We observe that the optimal number of phases is between 2 and 3. Only in the case of having efficiency as individual objective function (figure 158), it would be better to increase the number of phases up to 7 or 8, and select IGBT switches with lower power ratings.

Figure 156 Optimum number of phases - volume optimization
Figure 157 Optimum number of phases - Price optimization

Figure 158 Optimum number of phases - Efficiency optimization
7.1.1.3 Phase 1 Optimization results

Previous figures 141 to 158 show the evolution of different modulator performances and parameters for three individual objective functions: volume, efficiency and cost. This analysis makes possible to understand the sensitivity of each evaluated parameter to each individual objective function. However, in order to perform a global optimization, the objective function must include the three optimization parameters simultaneously, as shown in (95).

\[ f(x) = \text{Total}_{\text{Volume}} + \text{Total}_{\text{Losses}} + \text{Total}_{\text{Cost}} \]  

(95)

This objective function cannot be implemented directly in this way, as each of the three parameters have very different absolute values, which has an impact in the sensitivity of the objective function. To overcome this issue and assign the same function weight to each parameter, the maximum values of each parameter obtained during the individual objective function optimizations in 7.1.1.2, are introduced in the objective function as scaling factors, as shown in (96).

\[ f(x) = \frac{\text{Total}_{\text{Volume}}}{\text{Total}_{\text{Volume, max}}} + \frac{\text{Total}_{\text{Losses}}}{\text{Total}_{\text{Losses, max}}} + \frac{\text{Total}_{\text{Cost}}}{\text{Total}_{\text{Cost, max}}} \]  

(96)

Results of this optimization sweeps with this global objective function for different values of voltage droop in the main capacitor bank are presented in figures 159 to 163.
Figure 159 Total volume - Global optimization

Figure 160 PFS efficiency - Global optimization
Figure 161 Total cost - Global optimization

Figure 162 Operating cost for 20 years - Global optimization
Results of this global optimization sweeps show that two optimal voltage droop values exist for each IGBT technology: 1000 V for 1700 V, 1200 A IGBT switch technology, and 700 V for 1200 V, 600 A IGBT technology. This second option introduces more complexity due to the increase in the number of phases. In order to select the optimum solution between these two optimal voltage droop values for each IGBT switch technology, figure 164 shows the sum of the initial modulator cost and the 20 years operational cost. We observe that the minimum of the graph is exactly at 700 V for all IGBTs power ratings. This voltage droop value will be further studied in the second optimization phase described in 7.1.2, which considers the number of phases as a discrete variable.
7.1.2 Optimization Phase 2: optimal voltage, number of phases, and IGBT model

In this second optimization phase, further optimizations are performed considering a voltage droop in the main capacitor bank $C_{\text{max}}$ of 700 V, for different discrete values of number of phases. The linear and nonlinear inequality constraints follow the same structure presented on Figures 137 and 138, with the only difference that the number of phases is no longer an optimization variable, but a fixed input parameter for each optimization. In order to show consistency with previous optimization results obtained in 7.1.1, optimization sweeps for different discrete number of phases will be first performed on the same IGBT switches used in 7.1.1, and later only on 1200 V IGBT technology.

Figure 164 Sum of initial modulator cost and operational costs during 20 years - Global Optimization
Figure 165 shows the evolution of the volume as a function of the number of phases for different IGBT switches. The smallest modulator total volume is obtained for a 2-phases HCS active bouncer using 1200 V, 1200 A IGBTs; or 4-phases using 1200 V, 600 A IGBTs. Please notice that the jumps on the graphs are caused by a change in the number of phases value, which is now treated as a discrete variable. An integer change in this value has a direct impact on volume (number of IGBT modules) and switching frequency (equivalent switching frequency losses).

Figures 166 and 167 show the evolution of the pulse forming system efficiency and the total modulator price, as a function of the number of phases, respectively. We observe that the efficiency clearly decreases as the number of phases increase, and that the highest efficiency is achieved using 1200 V, 600 A IGBT technology. The price evolution is very similar to the one experienced by the modulator volume, and achieves its minimum for a 2-phases HCS active bouncer using 1200 V, 1200 A IGBTs; or 4-phases using 1200 V, 600 A IGBTs. The jumps in the graphs correspond again to changes in the number of phases (discrete variable).
Figure 166 PFS efficiency - Discrete Global optimization

Figure 167 Total price - Discrete Global optimization
Figure 168 shows the evolution of the operating cost corresponding to 20 years of operation as a function of the number of phases. The lowest cost is achieved for a single-phase HCS active bouncer using a 1200 V, 2400 A IGBT, or between 3 to 6 phases HCS using 1200 V, 600 A IGBTs.

![Figure 168 Operating cost during 20 years - Discrete Global optimization](image)

Finally, figure 169 shows the evolution of the sum of the initial modulator cost and the operation cost for a period of 20 years. We observe that the cost is minimized for a HCS Active Bouncer with 4 phases using 1200 V, 600 A IGBTs.
After demonstrating that 1200 V IGBT switch technology is more convenient for the HCS active bouncer, as previously shown in 7.1.1, new optimizations were performed for several commercial 1200 V IGBTs from Infineon. IGBTs presenting the lowest switching losses from each current ratings family were selected. Figures 170 to 174 present the evolution of the volume, PFS efficiency, total price, 20 years operating cost, and the sum of initial and operating cost. Results from these optimization sweeps show that the optimum modulator design from size, initial and operation cost, and volume point of view, is achieved for a 2-phases HCS active bouncer using FZ800R12KS4_BS 1200 V, 800 A IGBTs.

Figure 169 Initial and operating cost for 20 years - Discrete Global optimization
Figure 170 Volume - 1200V Discrete Global optimization

Figure 171 PFS efficiency - 1200V Discrete Global optimization
Figure 172 Total price - 1200V Discrete Global optimization

Figure 173 Operating cost 20 years - 1200V Discrete global optimization
7.1.3 Optimization Phase 3: correction and validation by numerical simulation

In this third and last design optimization step in the active bouncer HCS optimal design, performances of the optimal active bouncer design obtained using analytical models are compared with simulation results. The accuracy of the analytical models is improved using correction factors until a correct matching between analytical design models and simulation results is achieved. Convergence between the two models is achieved in just a few simulation iterations, which makes possible to reduce the computation time in comparison with a purely simulation based optimization approach, with the same accuracy.

Each correction factor, $k_c$, is computed at each iteration expression following expression (97).

$$k_c = \frac{Simulation\_value}{Analytical\_model\_value} \quad (97)$$
The performance parameter subject to correction in this particular design, is the output voltage pulse flat-top stability. There are two reason why different values of this performance parameter are expected. This first one is that the voltage stability precision is based on an open-loop transfer function frequency-domain gain analysis. The second one is that the simplified frequency-domain design models presented in 5.6 consider the klystron as a purely resistive load, and this hypothesis is only true for a given operating point. In fact, the klystron voltage and current follow the mathematical expression (98), where \( \tilde{I} \) stands for klystron perveance.

\[
I_{kly} = p \cdot V_{kly}^{3/2}
\]  

(98)

The simulation model, depicted on figure 175, uses this mathematical expression to model the klystron time-response.

The frequency-domain design model used, which is based on transfer functions, can only be applied to L.T.I. systems [122], and this is the reason for modelling the klystron as a purely resistive load. Figure 176 shows the waveforms of the optimal active bouncer design computed in 7.1.1. On this figure all waveforms follow exactly the expected behavior. The only difference is that the active bouncer presents a more abrupt reaction at the beginning to cope with the slower rise time response of the klystron in comparison with to a purely resistive load. However a zoom in the output voltage pulse, as shown on figure 177, shows that the output voltage pulse flat-top stability is actually 86 V, and not the expected 16.5 V corresponding to the requested 100 ppm.
Figure 176 Optimal analytical Active Bouncer waveforms: output voltage pulse, primary current, main capacitor bank voltage, and active bouncer output voltage
A correction factor has been successively applied to the output voltage stability design model described in 5.6. Figures 178 and 179 show the evolution of the correction factor value and the error of the parameter performance obtained by the analytical model in percentage. We observe that the correction factor convergence slightly oscillates around the final value during the first five iterations. This could be corrected by applying a smoothing factor \([138], \alpha\), with a value between 0 and 1, to the correction factor as shown in (99).

\[
k_c = \alpha \frac{\text{Simulation\_value}}{\text{Analytical\_model\_value}}
\]  

(99)

As shown on figure 179, the absolute error drops below 5\% after 5 numerical simulation iterations, below 1\% after just 7 iterations, and below 0.10\% after 10 iterations.
Figure 178 Evolution of the correction factor during 10 numerical simulation iterations

Figure 179 Evolution of the analytical model error in percentage during 10 numerical simulation iterations
The final optimal modulator design parameters are summarized in table 14.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cmain: $C_{\text{main}}$</td>
<td>295 µF</td>
</tr>
<tr>
<td>HCS number of phases: $N_{\text{phases}}$</td>
<td>2</td>
</tr>
<tr>
<td>HCS IGBT model</td>
<td>FZ800R12KS4_BS, 1200V, 800A</td>
</tr>
<tr>
<td>HCS diodes model</td>
<td>PN411211, 1200V, 1100A</td>
</tr>
<tr>
<td>HCS Inductance value per phase: $L_b$</td>
<td>704 µH</td>
</tr>
<tr>
<td>HCS output filter capacitance: $C_b$</td>
<td>4.6 µF</td>
</tr>
<tr>
<td>HCS output filter damping capacitance: $C_{\text{bd}}$</td>
<td>160 nF</td>
</tr>
<tr>
<td>HCS output filter damping resistance: $R_{\text{bd}}$</td>
<td>9.69 Ω</td>
</tr>
<tr>
<td>HCS switching frequency: $f_{\text{sw}}$</td>
<td>46 kHz</td>
</tr>
<tr>
<td>Heat-sink length: $HS_{\text{length}}$</td>
<td>0.72 m</td>
</tr>
<tr>
<td>Heat-sink width: $HS_{\text{width}}$</td>
<td>0.88 m</td>
</tr>
<tr>
<td>Heat-sink thickness: $HS_{\text{thickness}}$</td>
<td>0.08 m</td>
</tr>
<tr>
<td>Heat-sink fin height: $HS_{\text{fh}}$</td>
<td>0.18 m</td>
</tr>
<tr>
<td>Heat-sink fin thickness: $HS_{\text{ft}}$</td>
<td>0.017m</td>
</tr>
<tr>
<td>Heat-sink distance between fins: $HS_{\text{dtf}}$</td>
<td>0.03m</td>
</tr>
<tr>
<td>LS number of phases</td>
<td>4</td>
</tr>
<tr>
<td>LS MOSFET model</td>
<td>Ixys IXTK8N150L, 1500V, 8A</td>
</tr>
<tr>
<td>LS heatsink</td>
<td>Ohmite MA-302-55E</td>
</tr>
</tbody>
</table>

Figures 180 and 181 show the waveforms of the different modulator parameters, particularly the output voltage pulse, active bouncer output voltage, and current on each active bouncer phase. In 181 we can also see how the current in the linear stage reaches a maximum of 25 A.
Figure 180 Final optimal Active Bouncer waveforms: output voltage pulse, primary current, main capacitor bank voltage, and active bouncer output voltage
Figure 181 Final optimal Active Bouncer waveforms: output voltage pulse, active bouncer output voltage, current on HCS phase 1, current on HCS phase 2, and current on linear stage.
Figure 182 describes the thermal simulation model used to compute the linear MOSFETs junction temperature swing, which is depicted in figure 183.
Finally, Figure 184 shows a zoom on the modulator output voltage pulse, where we can observe that the 100 ppm output stability, corresponding to 16.5 V, is now respected.

\[ \Delta V = 16.4 \, \text{V} \]
7.2 Fast Voltage Compensator FVC

The optimal dimensioning of the FVC will be performed in a similar way as the active bouncer. However, due to the fact that the optimal voltage droop has already been identified in 7.1.1, the optimal design will consist of only two phases. During the first phase discrete optimization sweeps on FVC performances for discrete values of number of phases will be performed. This will allow to find the optimal IGBT switch model and number of phases. In the second and final phase numerical optimization results will be validated and corrected with numerical simulations.

The optimization problem design variables are listed in table 15, and the objective function would be the same as in the modulator optimization, given by (96).

<table>
<thead>
<tr>
<th>Design Variables</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{FVC}$</td>
<td>FVC inductance value (per phase)</td>
</tr>
<tr>
<td>$N_{phases}$</td>
<td>Number of phases</td>
</tr>
<tr>
<td>$C_d$</td>
<td>Capacitance on filter damping branch</td>
</tr>
<tr>
<td>$R_d$</td>
<td>Damping resistor on filter damping branch</td>
</tr>
<tr>
<td>$C_{fvc}$</td>
<td>FVC output filter capacitor</td>
</tr>
<tr>
<td>$F_{sw}$</td>
<td>FVC Switching frequency</td>
</tr>
<tr>
<td>$HS_{length}$</td>
<td>Heat sink length</td>
</tr>
<tr>
<td>$HS_{width}$</td>
<td>Heat sink width</td>
</tr>
<tr>
<td>$HS_{thickness}$</td>
<td>Heat sink thickness</td>
</tr>
<tr>
<td>$HS_{dtf}$</td>
<td>Heat sink distance between fins</td>
</tr>
<tr>
<td>$HS_{fh}$</td>
<td>Heat sink fin height</td>
</tr>
</tbody>
</table>

As in the case of the klystron modulator optimization, $A$, $b$, $A_{eq}$, $b_{eq}$ and $c_{eq}$ are null. Only lower and upper bounds are imposed for the design variables, and the maximum values for nonlinear constraints are directly derived from CLIC modulator specifications:

- Ripple amplitude on output voltage must not exceed 100 ppm in order to avoid introducing perturbations on charging current during the pulse.

- Minimum semiconductors lifetime must withstand 20 years of operation.

- Junction temperature on semiconductors must not exceed 125 °C.
• FVC open loop bandwidth (at -3 dB) must be higher than 7.1 kHz (frequency corresponding to CLIC pulse flat-top with, $1/t_{\text{flat}}$), in order to regulate a correct output voltage ramp during the pulse.

• Heat-sink surface must be bigger than the IGBTs baseplate surface.

7.2.1 Optimization phase 1: number of phases and IGBT switch model

Optimization sweeps have been performed to evaluate the optimum number of phases and switch technology. New IGBT switches with less current rating capability were selected, as the FVC charging current, computed using (7), is only 10.4 A. The lower current ratings allow for size, losses and cost reduction.

Figures 185, 186, 187 and 188 show the total FVC volume, efficiency, initial cost, and 20-year operating cost. The most compact and lowest cost FVC optimal design is achieved for a 1-phase H-bridge using 1200 V, 25 A IGBTs. However slightly higher efficiency, and therefore lower 20 year operating cost, is achieved with an FVC composed of 3 H-bridges using 1200 V, 15 A IGBTs.

![Figure 185 FVC Volume - Global Optimization](image-url)
Figure 186 FVC Efficiency - Global Optimization

Figure 187 Total FVC price - Global Optimization
Figure 189 clarifies the selection between the two optimal candidate solutions based on 25 A and 15 A IGBTs, by showing the sum of the initial cost and 20 year operating cost. The solution based on 1-phase H-bridge using FS25R12W1T4, 1200 V, 25 A IGBTs is the most compact (see previous figure 185) and presenting the lowest sum of initial and 20-years operating cost.
7.2.2 Optimization phase 2: correction and validation by numerical simulation

In this third and last design optimization step, the performances of the FVC analytical optimal solution verified using numerical simulation results. As previously performed in 7.1.3, correction factors will be introduced in order to improve the accuracy of the analytical models and reach convergence with simulation results. The simulation model used to verify the FVC performances is depicted in figure 190.
Figure 190 Optimal FVC simulation model

Figure 191 shows the simulated FVC waveforms. We can observe how the FVC correctly compensates for $C_{\text{main}}$ discharge, maintaining the charging voltage $V_{\text{CH}}$ constant. However, in figure 192 we observe a zoom on the charging voltage during the pulse, where one notices that the achieved voltage stability is 11.65 V, higher than the requested 2 V corresponding to the corresponding 100 ppm level of voltage stability required. This difference between predicted voltage stability by the frequency-domain design models and numerical simulation comes from the fact that the FVC current needs to perform almost an instantaneous step change between the current required during the charging phase (10), and the current during the pulsing phase (11). It is therefore a consequence of a transient response (settling time) to a step change in reference, as the frequency harmonics are damped to required voltage stability levels after few microseconds. Another factor that introduces a negative effect during this transient is the fact that the current during the pulsing phase is extremely low, causing the current in the FVC output filter inductor to go to discontinuous conduction mode (and therefore full DC bus voltage is applied to the output filter inductor, meaning maximum current slew rate) during the first 20 µs of the pulsing phase.
Figure 191 Optimal analytical FVC waveforms: charging voltage, main capacitor bank $C_{\text{main}}$ voltage, FVC output voltage, and FVC output current
To overcome this difference between analytical and numerical simulation results, a correction factor was applied to the output voltage stability nonlinear constraint. Figure 193 shows the evolution of the correction factor obtained using the analytical design models, in percentage. We can notice that the correction factor experienced even less slight oscillation around the final value than experienced in 7.1.1.3, although a smoothing factor (97) would introduce a subtle improvement in convergence speed. Figure 194 shows the evolution of the FVC voltage stability error in percentage with the numerical simulation correction steps. On Figure 194 we observe how the absolute errors drops below 5% after 4 numerical simulation iteration steps, and below 1% after 8 iteration steps.
Figure 193 Evolution of FVC correction factor during 10 numerical simulation iterations

Figure 194 Evolution of FVC analytical model error in percentage during 10 numerical simulation iterations
The final optimal FVC calculated design parameters are summarized in Table 16.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FVC number of phases: $N_{\text{phases}}$</td>
<td>1</td>
</tr>
<tr>
<td>FVC H-bridge IGBT model</td>
<td>FS25R12W1T4, 1200V, 25A</td>
</tr>
<tr>
<td>FVC Inductance value per phase: $L_{\text{FVC}}$</td>
<td>546 $\mu$H</td>
</tr>
<tr>
<td>FVC output filter capacitance: $C_{\text{FVC}}$</td>
<td>1.1 $\mu$F</td>
</tr>
<tr>
<td>FVC output filter damping capacitance: $C_{\text{FVCd}}$</td>
<td>3.9 $\mu$F</td>
</tr>
<tr>
<td>FVC output filter damping resistance: $R_{\text{FVCd}}$</td>
<td>1.24 $\Omega$</td>
</tr>
<tr>
<td>Pulsing phase switching frequency: $f_{\text{sw, pulse}}$</td>
<td>85.7 kHz</td>
</tr>
<tr>
<td>Charging phase switching frequency: $f_{\text{sw, ch}}$</td>
<td>6 kHz</td>
</tr>
<tr>
<td>Heat-sink length: $HS_{\text{length}}$</td>
<td>0.536 m</td>
</tr>
<tr>
<td>Heat-sink width: $HS_{\text{width}}$</td>
<td>0.916 m</td>
</tr>
<tr>
<td>Heat-sink thickness: $HS_{\text{thickness}}$</td>
<td>0.06 m</td>
</tr>
<tr>
<td>Heat-sink fin height: $HS_{\text{fh}}$</td>
<td>0.10 m</td>
</tr>
<tr>
<td>Heat-sink fin thickness: $HS_{\text{ft}}$</td>
<td>0.018m</td>
</tr>
<tr>
<td>Heat-sink distance between fins: $HS_{\text{dtf}}$</td>
<td>0.035m</td>
</tr>
</tbody>
</table>

Figure 195 shows the final FVC waveforms of the charging voltage, voltage droop of $C_{\text{main}}$, FVC output voltage and FVC output current. We can see that the current during the pulsing phase has increased its value, getting away of the discontinuous current conduction mode. Finally, figure 196 shows a zoom on the charging voltage, where we can see how the new design respects the 2 V voltage stability required.
Figure 195 Final optimal FVC waveforms: charging voltage, primary current, main capacitor bank voltage, FVC output voltage, and FVC output current
As a conclusion to this chapter, the global optimal design method introduced in chapter 3 has been successfully applied to the optimal dimensioning of a full-scale modulator equipped with the proposed SPDC topology (Active Bouncer and SPDC) respecting CLIC specifications. Due to the need to take into account discrete variables, like number of phases or IGBT switch technology, an optimization approach in three phases has been adopted. The first phase identified the optimal size of the modulator capacitor bank, $C_{\text{main}}$, and therefore the voltage droop that has be compensated by the SPDC active bouncer. The second phase identified the optimal IGBT switch technology and number of phases. And finally, in the third phase a full optimization procedure which included the correction of the analytical design models by analytical simulation results until convergence was performed in order to improve the accuracy and validate the final optimization results.

Figure 196 Final optimal FVC: Zoom on charging voltage during a pulse discharge

\[\Delta V = 1.995 \, \text{V}\]
CONCLUSION AND FUTURE WORKS

This dissertation addressed the optimal design of high performance pulsed power converters and, in particular, the design of a klystron modulator for CLIC. The main scientific contributions of this research work can be summarized as:

- Two novel klystron modulator topologies based on a monolithic step-up pulsed transformer able to perform active voltage droop compensation and, at the same time, make possible a constant power consumption operation from the grid. The first one, DPAB, more interesting for high average power and long pulse applications. The second one, SPDC, more interesting from the efficiency and performances point of view, for short-pulse applications like CLIC.

- Novel active bouncer topology using a high-current low-frequency stage in combination with a low-current high-bandwidth linear stage, achieving the lowest possible losses while guaranteeing high-bandwidth to correctly compensate the voltage droop for short-pulse applications, when high dynamics is required.

- Application of Space Mapping Techniques to Power Electronics Design. The proposed global optimal design methodology applies nonlinear optimization algorithms to analytical design models, previously validated experimentally, and correction using numerical simulations. Convergence is achieved in less than 10 numerical simulation iterations, making possible to achieve the same results in terms of accuracy as pure optimizations using numerical simulation but at the same time, requiring much less computational time and power.

- Complete optimal design of full-scale klystron modulator for CLIC, including active bouncer HCS and LS stages, and FVC. Clarification of optimal voltage droop (main capacitor bank value), power converters topology and design parameters.

- Successful experimental validation of proposed active bouncer and FVC topologies using reduced-scale prototypes.

Research work presented in this dissertation, has also been presented and published in several international IEEE conferences and journals [97][110][122][123][124][125][126].

214
The objectives of this research work, presented in 1.3, have been fulfilled. Nonetheless, there is still room for future works, mainly in three different areas:

- **New semiconductor technologies**: New semiconductor technologies, like SiC MOSFETs [133] could be a more interesting alternative to Si IGBTs to achieve higher efficiency and higher performances due to their higher switching frequency capabilities for the FVC. However, information regarding power cycling impact on these devices is not yet available. This technology could also be interesting for the SPDC HCS in order to achieve a higher efficiency design, however this would require the utilization of a high number of SiC MOSFETs due to the fact that only discrete relatively low power modules are available, which could have a negative impact in reliability.

- **Control**: Multiphase interleaving hysteretic current and voltage controllers have been applied to the SPDC power converters in this dissertation due to their high dynamics and bandwidth response. However, due to the fact that the HCS and FVC must produce ramps at its output, fixed hysteresis bands produce varying switching frequency actuations during the ramps. This introduces the additional complexity on how to interleave different phases when the switching frequency is continuously varying, for which a solutions has still not been published in the literature. Another control aspect that could be studied in the future is the active damping of the HCS harmonics using the LS by pulse-to-pulse closed-loop control or precomputed waveforms.

- **Power compensation**: The FVC could have interesting application in many other applications, like industrial chargers, diesel generators in aircraft-carriers for fighter planes launchers, and almost any high power capacitor discharge application requiring to reduce peak power consumption from the utility grid.
References


[76] L. Amoroso, M. Donati, « Single Shot TransientSuppressor (SSTS) for High Current High Slew Rate Microprocessor », APEC 1999 IEEE.


References


References


ANNEX A

A. Fine inductance dimensioning model

In this annex, the magnetics design models to estimate the equivalent inductance, maximum current value before saturation, magnetic and copper losses, total mass and volume, for a given inductance geometrical parameters and number of turns are presented. These models were used to verify the inductor fitting models presented in 5.4. The inductor topological structure considered in this dimensioning model is made of two E standard shape magnetic cores with an air-gap e, as shown on figure 197. The inductor winding configuration consists in two series connected coils that are wounded around the core external columns.

Several simplifying assumptions have been adopted in this dimensioning model:

- Detailed skin effect and proximity effects are not fully considered in the estimation of the copper losses. The systematic use of Litz wire is supposed to minimize their influence.

- Isolation distances between magnetic core and coils are neglected, because this application concerns low voltage inductors with their magnetic core connected to ground potential.

- Flux fringing at the air-gap level is neglected.

- Magnetic saturation is not considered for magnetic induction levels under the maximum magnetic induction value $B_{\text{max}}$ selected from the magnetic material characteristics ($B_{\text{max}}$ is an input variable of the design tool and imposed by the user). One considers that the material magnetic permeability is constant under $B_{\text{max}}$.

The inductance design can be divided in three phases: inductance calculation, losses estimation, and thermal validation.
1 Inductance calculation

The calculation of the inductance value corresponding to the inductor structure, depicted on figure 197, is performed using its equivalent magnetic circuit shown on figure 198 A). The different reluctance values are calculated from the geometry and the core material parameters. The inductance value is derived from these reluctances and the number of turns $N$ of each single coil that are connected in series.

Figure 198 Equivalent magnetic circuit of the inductance. A) Complete circuit; B) Simplified circuit
In order to compute the equivalent circuit reluctance values, the area of the external magnetic core columns $A_{ec}$ and the area of the central column $A_{cc}$ can be calculated as shown in (100) and (101), respectively.

$$A_{ec} = c \cdot d$$  \hspace{1cm} (100)

$$A_{cc} = 2 \cdot c \cdot d$$  \hspace{1cm} (101)

The different reluctance values of the equivalent circuit depicted on figure 198.A, where $F = NI_{calc}$, are therefore:

$$R_{ec} = \frac{2a+b+4c}{\mu A_{ec}}$$  \hspace{1cm} (102)

$$R_{cc} = \frac{b+c}{\mu A_{cc}}$$  \hspace{1cm} (103)

$$R_{ecg} = \frac{e}{\mu \sigma A_{ec}}$$  \hspace{1cm} (104)

$$R_{ccg} = \frac{e}{\mu \sigma A_{cc}}$$  \hspace{1cm} (105)

The total reluctance is calculated considering the equivalent simplified circuit depicted on figure 198.B as follows:

$$R_{tot} = \frac{R_{ec} + R_{ecg}}{2} + R_{cc} + R_{ccg}$$  \hspace{1cm} (106)

The inductance value can be now computed, using the expression (107):

$$L_{calc} = \frac{N^2}{R_{tot}}$$  \hspace{1cm} (107)

The maximum current value $I_{calc}$ that would lead to saturation of the magnetic core for a given maximum magnetic induction value $B_{max}$, using Ampère theorem:

$$\Phi = B_{max} \cdot A_{cc}$$  \hspace{1cm} (108)

$$I_{calc} = \frac{R_{tot} \Phi}{N}$$  \hspace{1cm} (109)
2 Inductance losses estimation

Two different types of losses in the inductance are considered: copper losses in the windings and magnetic losses in the core.

The copper resistivity value $\rho_{Cu}$ is considered constant. Its value is computed from the maximum copper temperature $T_{Cu, max}$, and imposed by the specified value of the temperature rise, which is an inductor design constraint:

$$\rho_{Cu} = 1.724 \times 10^{-8} \left[ 1 + 0.004 \left( T_{Cu, max} - 20 \right) \right]$$  \hspace{1cm} (110)

From the inductance structure, one can derive the mean length per turn $MLT$, the total cross-section of one of the two external copper coils $S_{Cu}$, and the total volume of copper in the two series connected coils as follows:

$$MLT = 2 \left( 2a + c + d \right)$$  \hspace{1cm} (111)

$$S_{Cu} = K_{Cu} \cdot a \cdot b$$  \hspace{1cm} (112)

$$V_{Cu} = 2 \cdot MLT \cdot S_{Cu}$$  \hspace{1cm} (113)

The RMS value of the current in the inductance $I_{RMS}$ can be calculated from the periodic instantaneous current waveform on a steady state cycle of operation of the application (in our specific case concerning the active bouncer, it is derived from the output filter values and the number of phases), leading to a corresponding RMS current density:

$$J_{RMS} = \frac{N \cdot I_{RMS}}{2 \cdot S_{Cu}}$$  \hspace{1cm} (114)

With this value, the copper losses can be finally calculated using expression (115):

$$P_{Cu} = \rho_{Cu} \cdot V_{Cu} \cdot J_{RMS}^2$$  \hspace{1cm} (115)

Regarding the magnetic losses they are evaluated from the inductor core volume and the magnetic losses volumetric density by applying the improved generalized Steinmetz equation (iGSE) [109].
3 Inductance Thermal Modelling

A simplified inductance thermal model is used to calculate the temperature of copper coils and magnetic core. The following simplifications are considered:

- Temperatures in the copper coils \( T_{Cu} \) an in the magnetic core \( T_{Core} \) present a homogenous distribution.

- There is no heat exchange between magnetic core and coils. The individual temperature increase is only due to magnetic losses and copper losses, respectively.

- Heat transfer coefficient for convection and radiated heat dissipation remains constant in the temperature range considered (40 °C to 150 ºC). Only natural convection is considered as a conservative approach.

- Internal copper temperature is estimated to be 15 °C higher than the temperature on the external surface of the coils which are in contact with air.

- Heat dissipation is only considered for the surfaces in direct contact with air. Heat dissipation in contact surfaces between core and coils is not considered.

The total copper and magnetic core external surfaces in contact with air can be calculated using the following expressions:

\[
S_{Cu,Ext} = 4. b. (4. a + c) + 4. [(2. a + c). (2. a + d) − c. d]
\]  
(116)

\[
S_{Core,Ext} = 4. l_{mag}. c + 4. b. c + 4. c. d + 2. l_{mag}. d
\]  
(117)

The temperature on the magnetic core surface \( T_{Core,Ext} \), copper coils surface \( T_{Cu,Ext} \) and internal copper coils layers \( T_{Cu} \) can be estimated using the previously calculated magnetic and copper losses as follows:

\[
T_{Cu,Ext} = T_{amb} + \frac{P_{Cu}}{h_{Diss}S_{Cu,Ext}}
\]  
(118)

\[
T_{Cu} \approx T_{Cu,Ext} + 15
\]  
(119)

\[
T_{Core,Ext} = T_{amb} + \frac{P_{mag}}{h_{Diss}S_{Core,Ext}}
\]  
(120)
As a final step, the total mass (sum of the mass of magnetic material $M_{\text{Core}}$ and the mass of copper $M_{\text{Cu}}$), the magnetic energy stored in the inductance $W_{\text{mag}}$ and the coils wire copper section $S_{\text{wire}}$ are calculated:

$$M_{\text{Core}} = \rho_{\text{Core}} \cdot V_{\text{mag}, \text{total}}$$

$$M_{\text{Cu}} = \rho_{\text{Cu}} \cdot V_{\text{Cu}}$$

$$M_{\text{Total}} = M_{\text{Core}} + M_{\text{Cu}}$$

$$W_{\text{mag}} = \frac{l_{\text{calc}}^2 \cdot \text{calc}^2}{2}$$

$$S_{\text{wire}} = \frac{2 \cdot S_{\text{Cu}}}{N}$$

4 Inductance volume

The inductance volume can be calculated from the magnetic core dimensions and filling factor coefficient:

$$V_{\text{ind}} = (2 \cdot a + 4 \cdot c + 2 \cdot k_{\text{u}} \cdot a) \cdot (d + 2 \cdot k_{\text{u}} \cdot a) \cdot (b + 2 \cdot c)$$

5 Fine model application example

In order to validate the approach used in the Power Electronics Design Tool of using a simplified inductor model, the fine inductance dimensioning model is here applied to the calculated active bouncer optimal inductance of Table 14. The characteristics of this inductance are summarized again in Table 17.

<table>
<thead>
<tr>
<th>Table 17 Active Bouncer HCS inductance parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>HCS Inductance value: $L_b$</td>
</tr>
<tr>
<td>Maximum current in inductance: $I_{\text{max}}$</td>
</tr>
<tr>
<td>RMS current value in inductance: $I_{\text{RMS}}$</td>
</tr>
</tbody>
</table>

An optimal inductance geometry that respects these specifications having as objective function to minimize the total inductor mass has been calculated and it is shown on figure 199.
Applying iGSE to this inductor geometry and operating mode, the total average magnetic losses during the pulse are 15 W, and the temperatures on the copper and on the inductance core are summarized in Table 18. The copper temperature remains below 75ºC and the core temperature below 60ºC. Even considering 450% higher magnetic losses, the temperature in the copper remains still below 75ºC and the core temperature below 120ºC. This is because for this specific inductance parameter and pulsed application, the inductor core volume is imposed by the peak value of magnetic energy stored without saturation in the inductor at $I_{\text{max}}=720$ A. This volume imposed by the peak magnetic energy value leads to a very conservative heat dissipation surface which is very efficient in terms of steady-state copper and core temperature with a RMS current equal to 46 A only. We can therefore state in this specific case the magnetic losses have little influence in the inductance design, and therefore can be neglected.

**Table 18 Temperature on HCS optimal inductance**

<table>
<thead>
<tr>
<th>Nominal magnetic losses</th>
<th>450 times higher magnetic losses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper temperature</td>
<td>72.2ºC</td>
</tr>
<tr>
<td>Core temperature</td>
<td>59.8ºC</td>
</tr>
<tr>
<td>Copper temperature</td>
<td>72.2ºC</td>
</tr>
<tr>
<td>Core temperature</td>
<td>119.3ºC</td>
</tr>
</tbody>
</table>
The PFS global efficiency has been calculated using the following expression:

\[
\eta_{PFS} = \frac{P_{\text{mod.out}}}{P_{\text{PFS,in}}} = \frac{P_{\text{mod.out}}}{P_{\text{mod.out}} + P_{\text{HCS}} + P_{\text{LL}} + N_{\text{phases}} \cdot (P_{\text{Cu}} + P_{\text{mag}})}
\]  

(157)

Where \(P_{\text{HCS}}\) are the losses in the Active Bouncer high current stage, \(P_{\text{LL}}\) the losses in the linear stage, \(N_{\text{phases}}\) the number of phases, \(P_{\text{Cu}}\) the copper losses on each inductor, and \(P_{\text{mag}}\) the magnetic losses also on each inductor. Table 19 shows the PFS efficiency obtain with the calculated magnetic losses, and also considering 10 times higher magnetic losses. Even in this last scenario, the CLIC PFS efficiency specification of Table 1 (0.98) is still respected. We can therefore state that the magnetic losses in the inductances have also little influence in the pulse forming system efficiency, and therefore also in the global modulator efficiency, and they can be neglected in the Power Electronics System Dimensioning Tool.

### Table 19 Pulse forming system efficiencies

<table>
<thead>
<tr>
<th></th>
<th>Nominal magnetic losses</th>
<th>10 times higher magnetic losses</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\eta_{PFS})</td>
<td>0.9934</td>
<td>0.9928</td>
</tr>
</tbody>
</table>